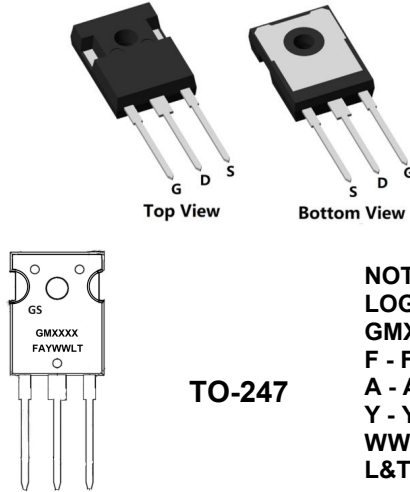


N-Channel 650V, 70mΩ max, Super Junction MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
650	70 @ $V_{GS} = 10V$	47 ⁽¹⁾

View and Internal Schematic Diagram



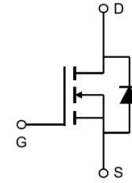
Features

- Low $R_{DS(on)}$ and Fom
- Low Switching loss
- 100% avalanche tested. High avalanche ruggedness
- Excellent stability and uniformity

Application

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- UPS / Solar (PV inverters)
- Induction heating
- Motor driver
- Battery chargers

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ⁽¹⁾	I_D	47	A
		30	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	188	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	810	mJ
Power dissipation	P_D	357	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.35	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient	$R_{\theta JA}$	40	

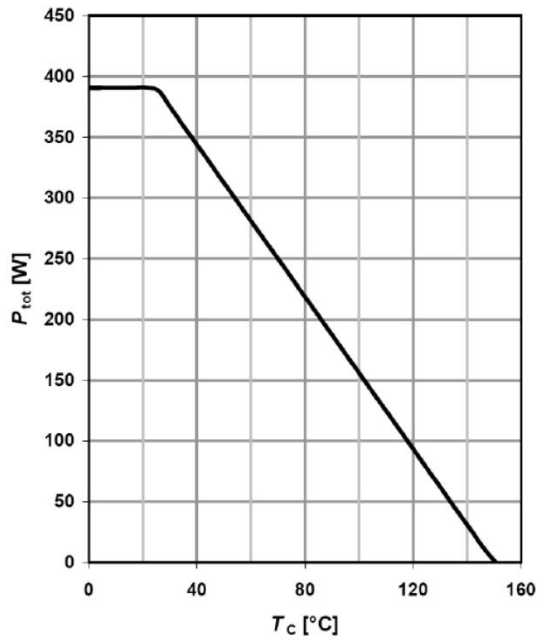
Electrical characteristics (Ta=25°C ± 3°C)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	650			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 mA	3	4	5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±30 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		62	70	mΩ
Gate resistance	R _g	f = 1 MHz, open drain		0.03		Ω
Dynamic ⁽⁴⁾						
Total gate charge	Q _g	V _{DS} = 400 V, I _D = 17 A, V _{GS} = 10 V		76.3		nC
Gate-source charge	Q _{gs}			22		
Gate-drain charge	Q _{gd}			25.7		
Turn-on delay time	t _{d(on)}	V _{DS} = 400 V, I _D =10 A, V _{GS} = 10 V, R _{GEN} = 2 Ω		21		ns
Rise time	t _r			11		
Turn-off delay time	t _{d(off)}			92		
Fall time	t _f			7		
Input capacitance	C _{iss}	V _{DS} = 400 V, V _{GS} = 0 V, f = 100 KHz		4096		pF
Output capacitance	C _{oss}			84		
Reverse transfer capacitance	C _{rss}			8		
Reverse Diode Characteristics ⁽⁴⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 17 A		0.9	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 100 V,I _F = 10 A, di/dt = 100 A/μs		720		ns
Reverse recovery charge	Q _{rr}			15		uC

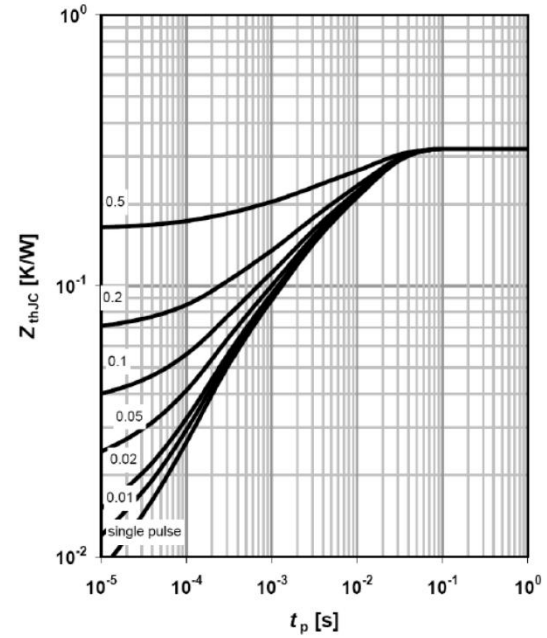
Notes

- (1) Limited by maximum junction temperature.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 130\text{ V}, V_{GS} = 10\text{ V}, L = 60\text{ mH}$.
- (4) Guaranteed by design, not subject to production testing.

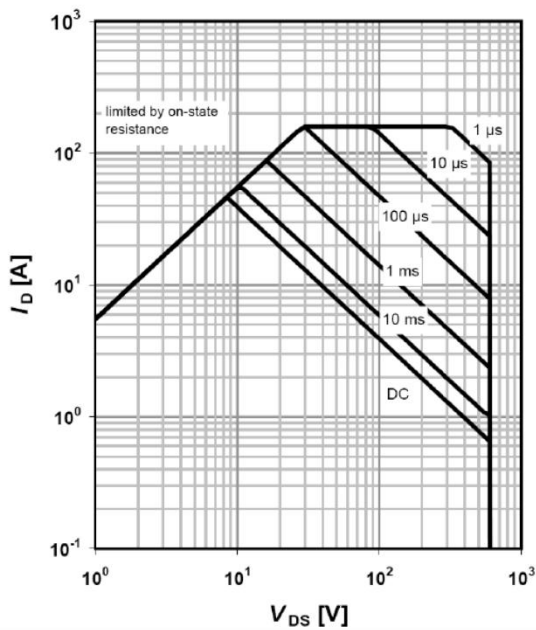
Typical Performance Characteristics

Power dissipation


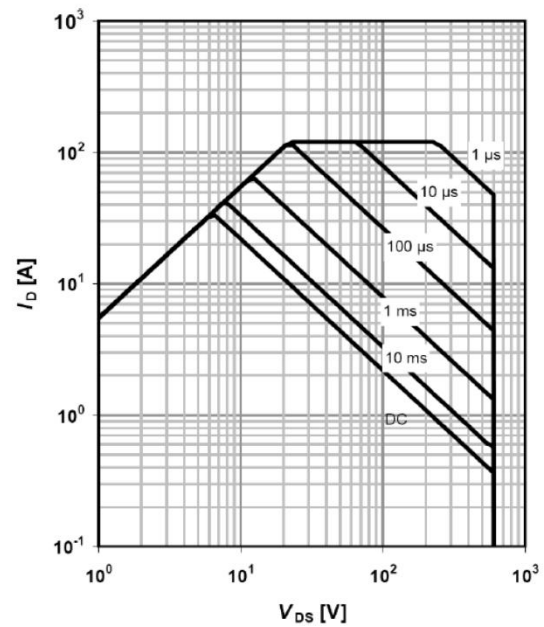
$$P_{\text{tot}} = f(T_c)$$

Max. transient thermal impedance


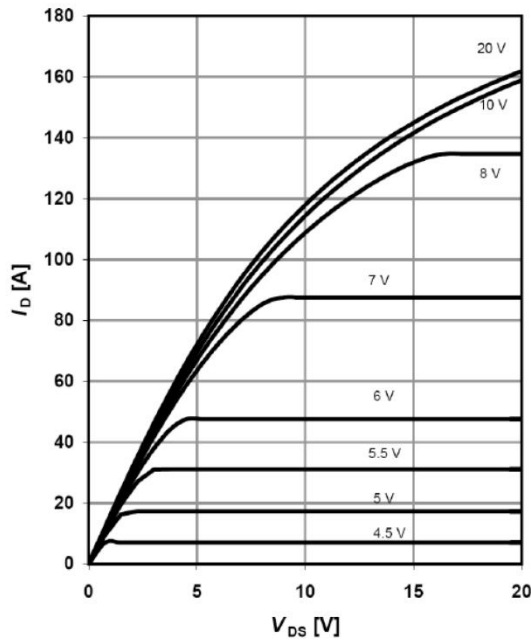
$$Z_{\text{thJC}} = f(t_p); \text{ parameter: } D = t_p/T$$

Safe operating area $T_c = 25^\circ\text{C}$


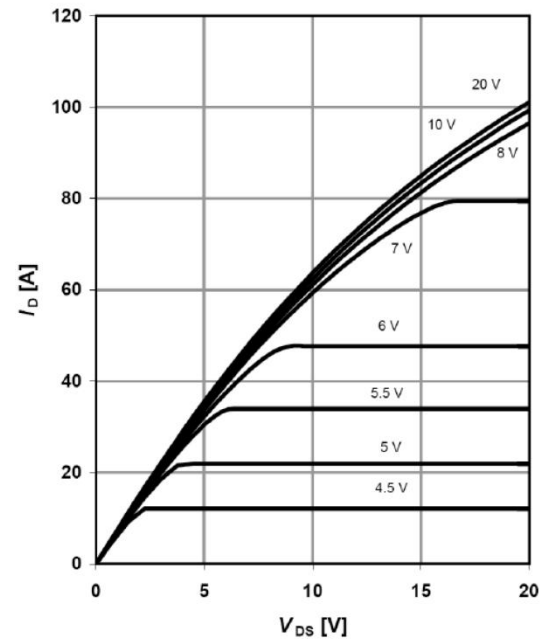
$$I_D = f(V_{DS}); T_c = 25^\circ\text{C}; V_{GS} > 7\text{V}; D = 0; \text{ parameter } t_p$$

Safe operating area $T_c = 80^\circ\text{C}$


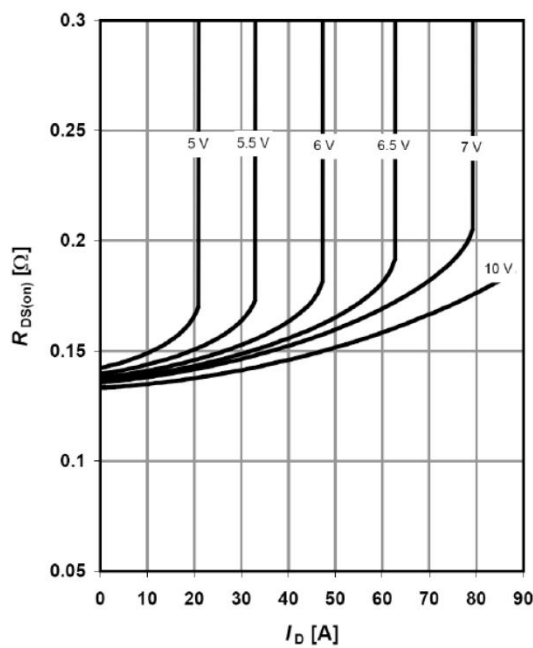
$$I_D = f(V_{DS}); T_c = 80^\circ\text{C}; V_{GS} > 7\text{V}; D = 0; \text{ parameter } t_p$$

Typ. output characteristics $T_j=25\text{ }^{\circ}\text{C}$


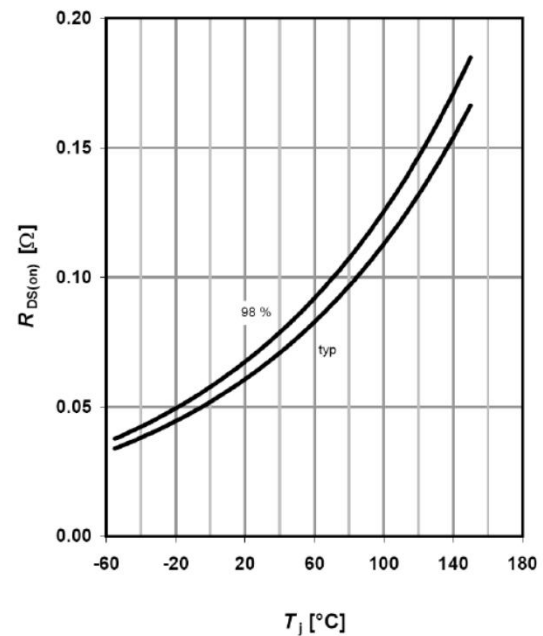
$$I_D = f(V_{DS}); T_j = 25\text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$$

Typ. output characteristics $T_j=125\text{ }^{\circ}\text{C}$


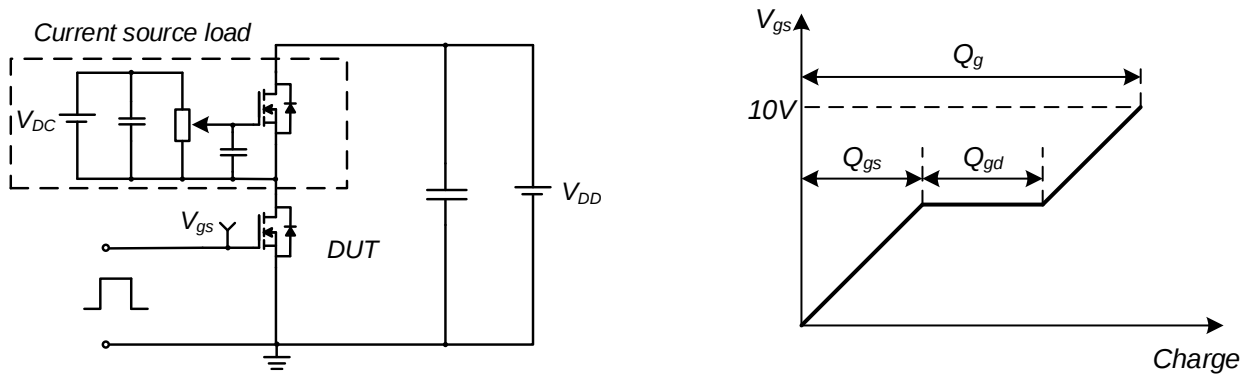
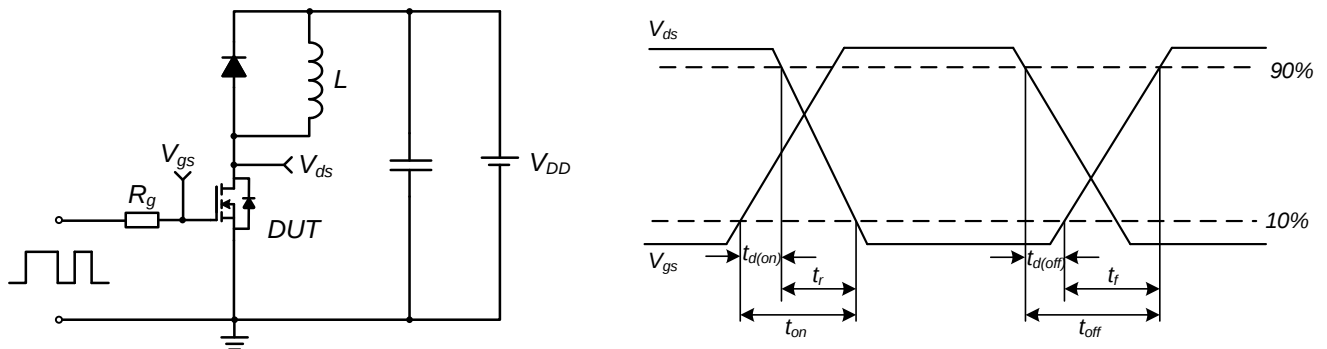
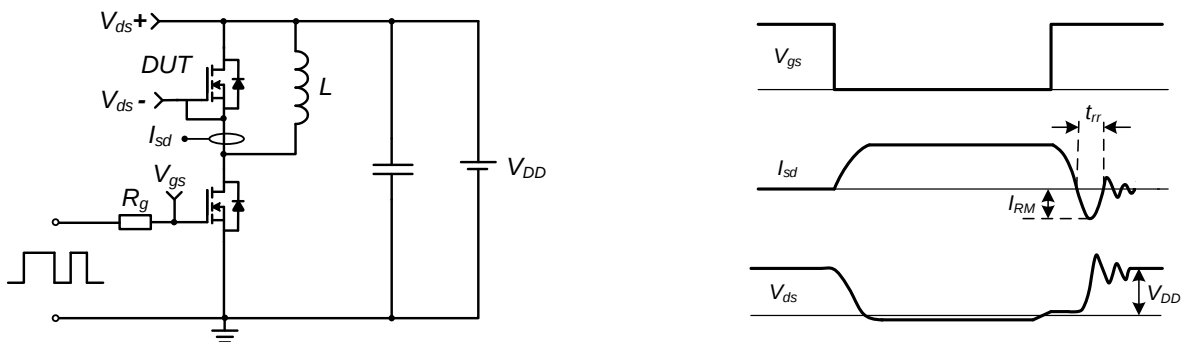
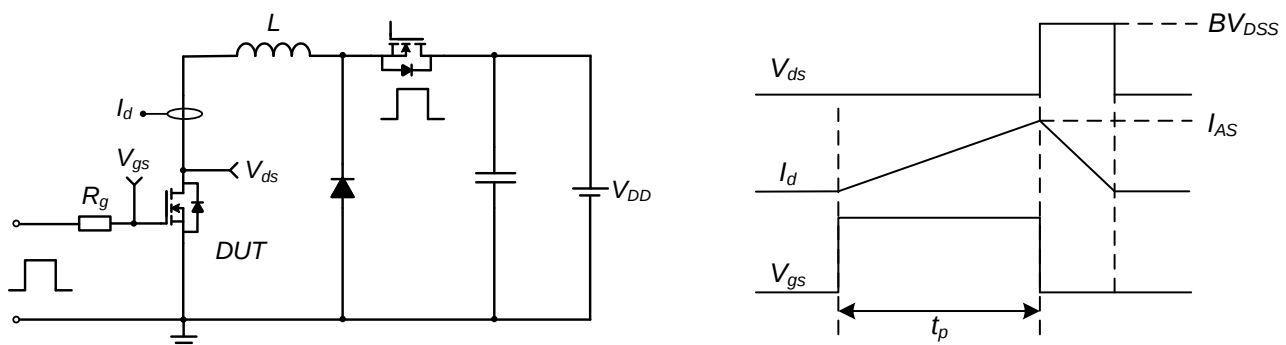
$$I_D = f(V_{DS}); T_j = 125\text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$$

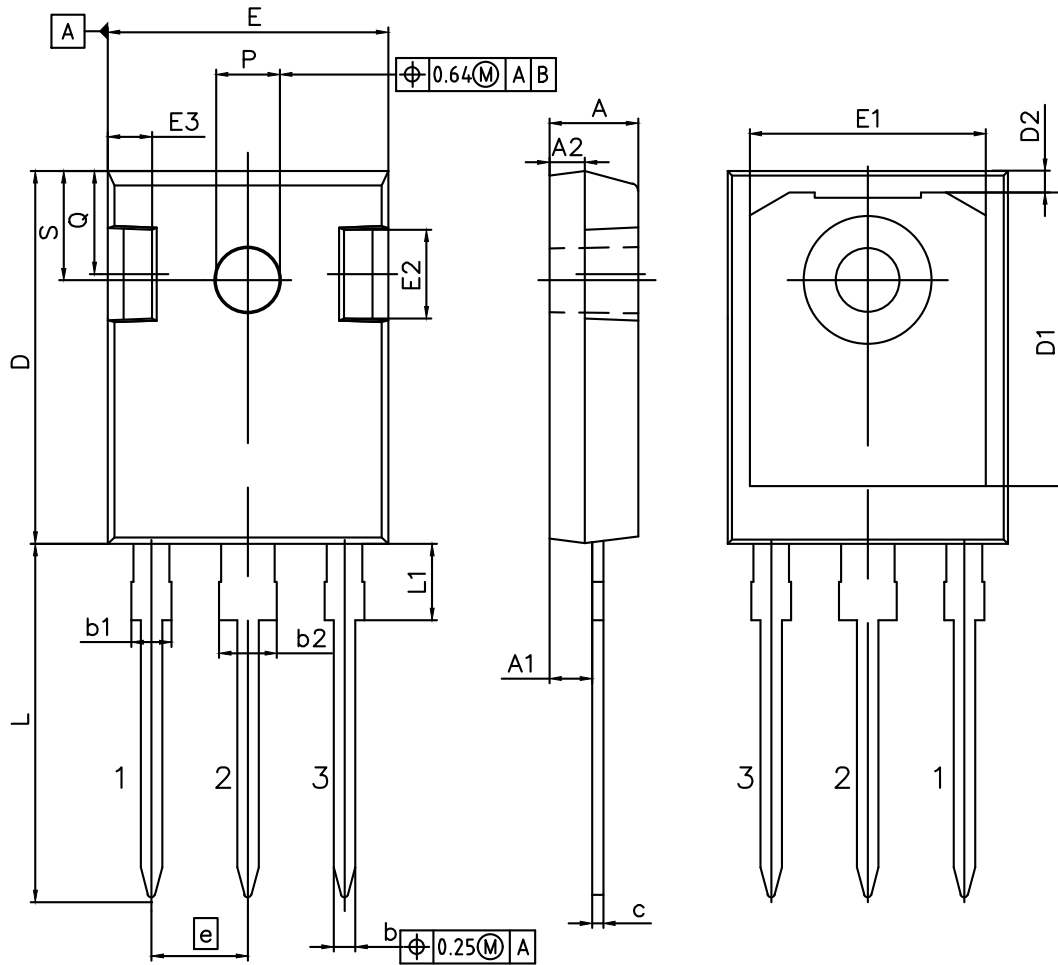
Typ. drain-source on-state resistance


$$R_{DS(on)} = f(I_D); T_j = 125\text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$$

Drain-source on-state resistance


$$R_{DS(on)} = f(T_j); I_D = 17.6\text{ A}; V_{GS} = 10\text{ V}$$

Test Circuits & Waveforms
Figure 14. Gate charge test circuit & waveforms

Figure 15. Switching time test circuit & waveforms

Figure 16. Diode reverse recovery test circuit & waveforms

Figure 17. Unclamped inductive switching test circuit & waveforms


Package outline dimensions: TO-247


DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
L	19.80	20.40
L1	3.85	4.50
P	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

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