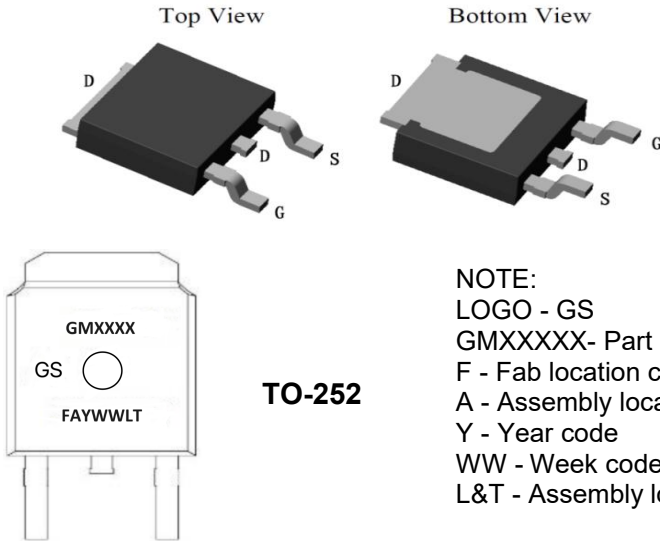


N-Channel 700V,900mΩ max,Super Junction MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
700	900 @ $V_{GS} = 10V$	6 ⁽¹⁾

View and Internal Schematic Diagram



NOTE:
 LOGO - GS
 GMXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

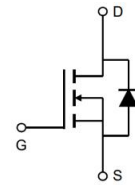
Features

- Low $R_{DS(on)}$ and Fom
- Low Switching loss
- 100% avalanche tested. High avalanche ruggedness
- Excellent stability and uniformity

Application

- LED/LCD/PDP TV and monitor Lighting
- Solar/Renewable/UPS-Micro Inverter System
- Charger
- Power Supply

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	700	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ⁽¹⁾	I_D	6	A
		4	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	22	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	60	mJ
Power dissipation	P_D	71	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	1.76	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient	$R_{\theta JA}$	134	

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	700			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	3		4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			±100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		780	900	mΩ
Gate resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		9		Ω
Dynamic⁽⁴⁾						
Total gate charge	Q_g	$V_{DS} = 480\text{ V}, I_D = 3\text{ A}, V_{GS} = 10\text{ V}$		11		nC
Gate-source charge	Q_{gs}			3.2		
Gate-drain charge	Q_{gd}			4.5		
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 400\text{ V}, I_D = 3\text{ A}, V_{GS} = 10\text{ V},$ $R_{GEN} = 27\text{ }\Omega$		13		ns
Rise time	t_r			14		
Turn-off delay time	$t_{d(off)}$			51		
Fall time	t_f			60		
Input capacitance	C_{iss}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ M Hz}$		325		pF
Output capacitance	C_{oss}			32		
Reverse transfer capacitance	C_{rss}			1.2		
Reverse Diode Characteristics⁽⁴⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = 3\text{ A}$		0.85	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 100\text{ V}, I_F = 3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		186		ns
Reverse recovery charge	Q_{rr}			1.45		μC

Notes

- (1) Limited by maximum junction temperature.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, L = 30\text{ mH}$.
- (4) Guaranteed by design, not subject to production testing.

Typical Performance Characteristics

Fig 1. Output Characteristics ($T_j=25^\circ\text{C}$)

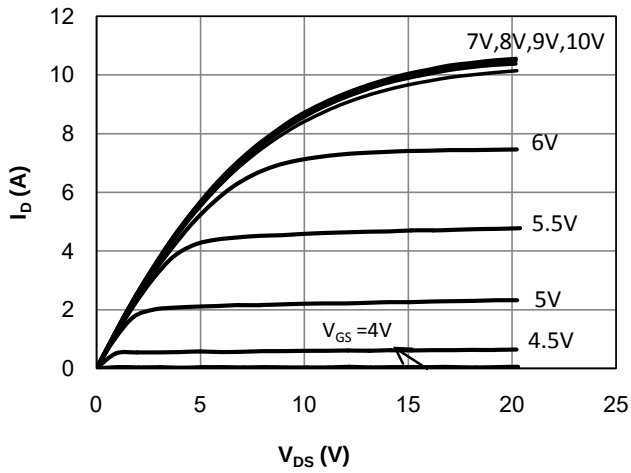


Fig 2. Output Characteristics ($T_j=150^\circ\text{C}$)

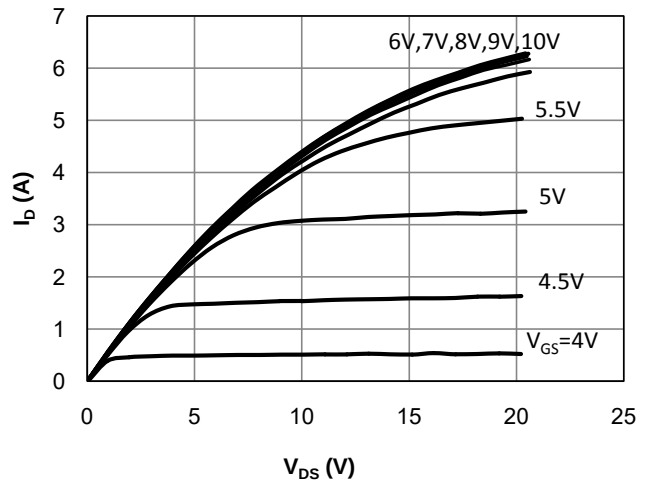


Fig 3: Transfer Characteristics

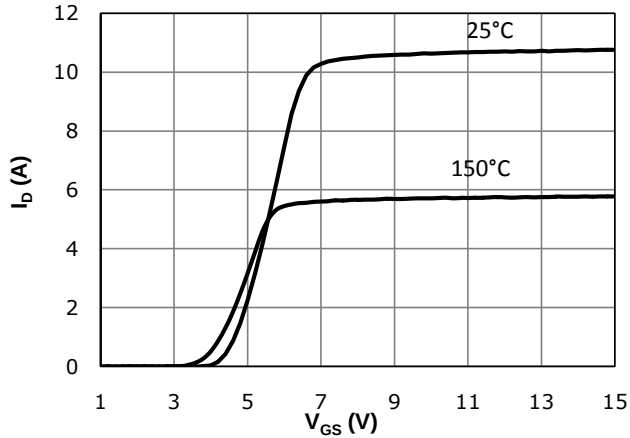


Fig 4: V_{TH} vs. T_j Temperature Characteristics

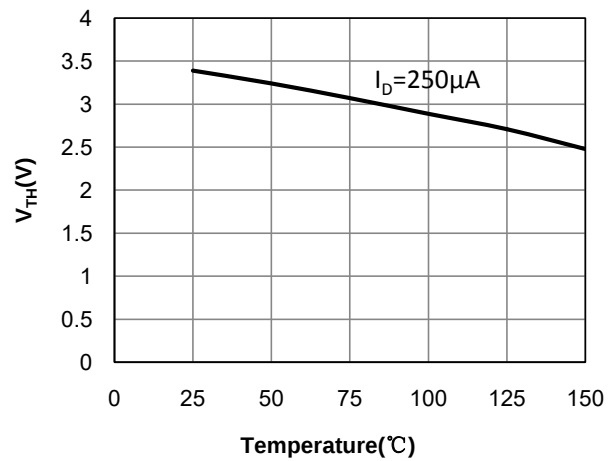


Fig 5: $R_{DS(on)}$ vs. I_{DS} Characteristics ($T_j=25^\circ\text{C}$)

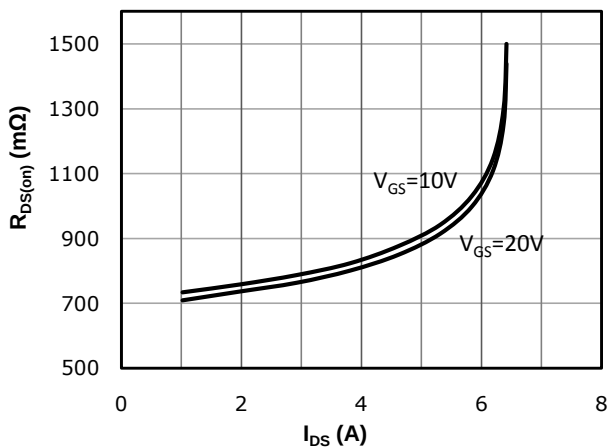
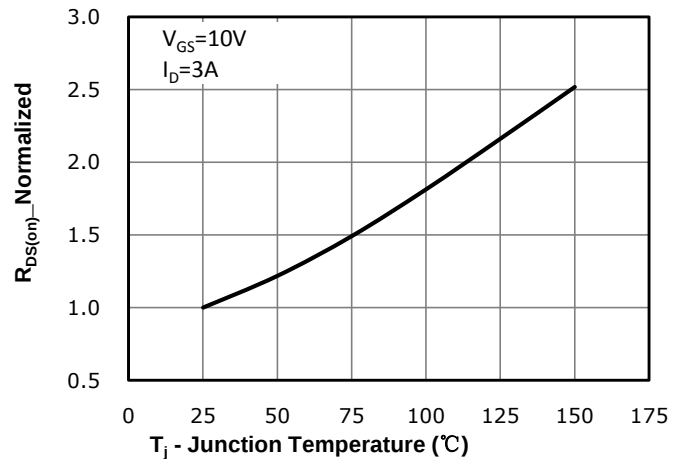


Fig 6: $R_{DS(on)}$ vs. Temperature



Typical Performance Characteristics

Fig 7: BV_{DSS} vs. Temperature

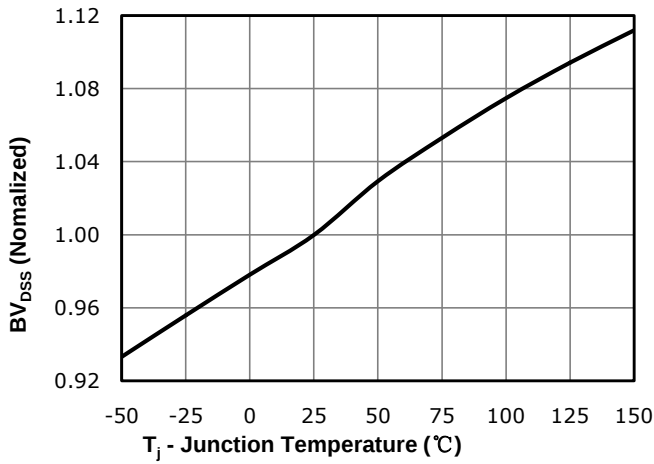


Fig 8: $R_{DS(on)}$ vs. Gate Voltage

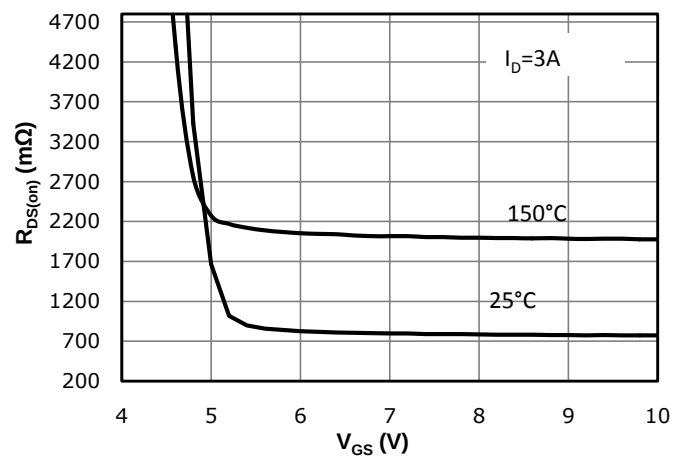


Fig 9: Body-diode Forward Characteristics

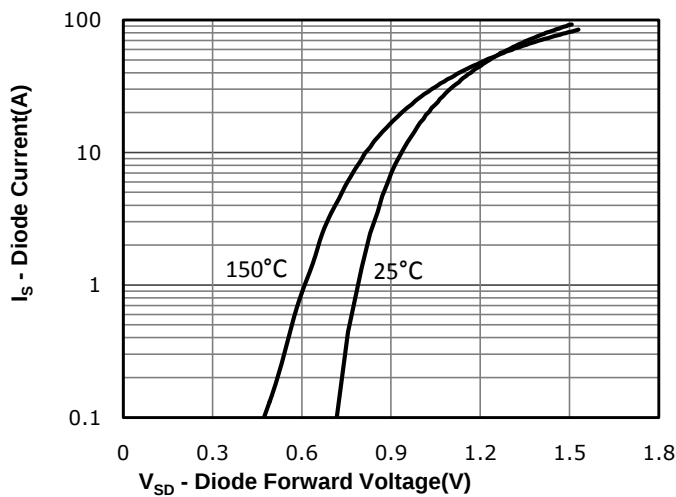


Fig 10: Gate Charge Characteristics

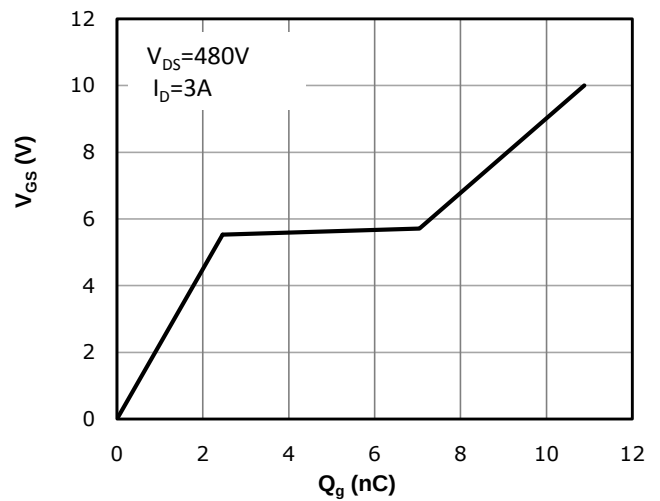


Fig 11: Capacitance Characteristics

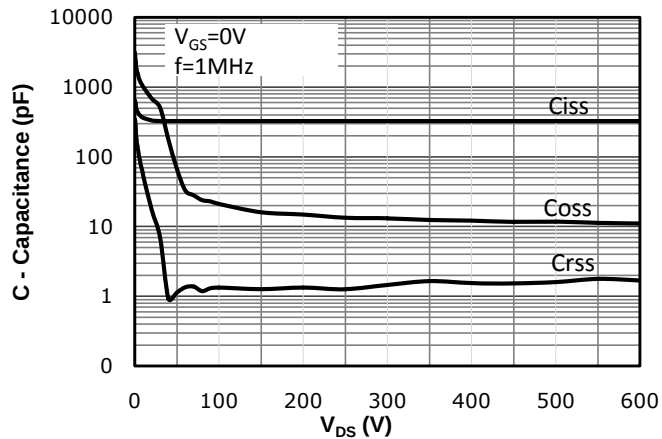
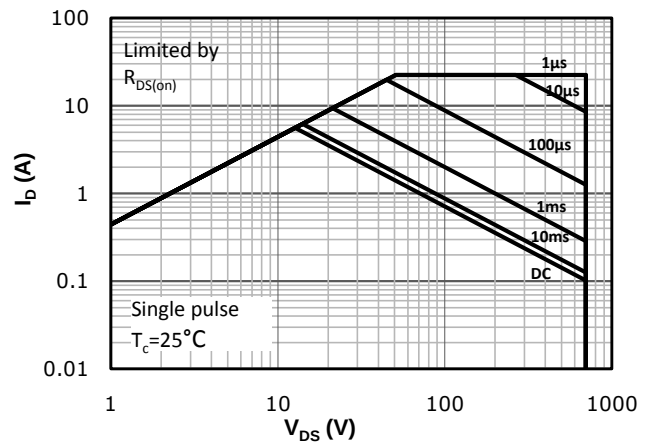
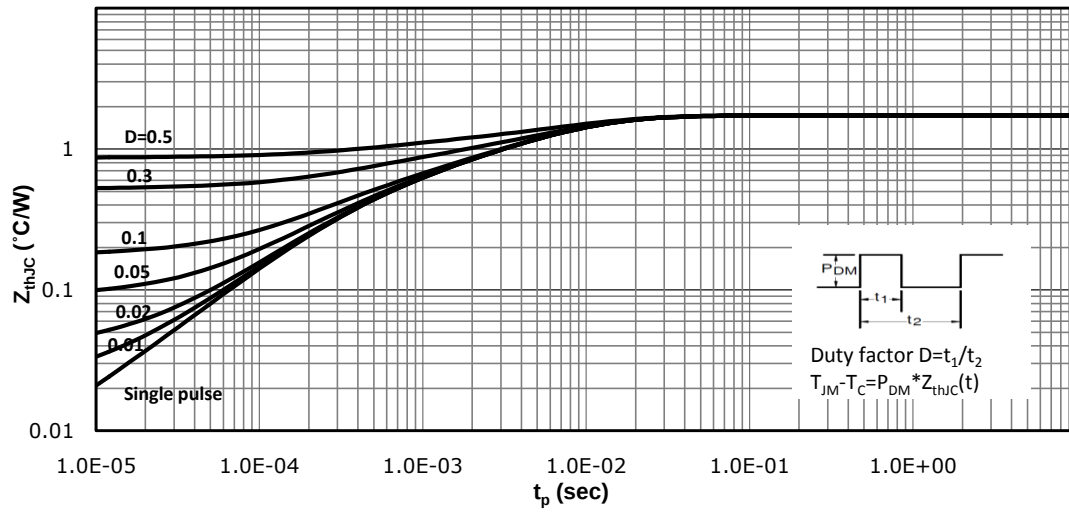


Fig 12: Safe Operating Area



Typical Performance Characteristics
Fig 13: Max. Transient Thermal Impedance


Test Circuits & Waveforms

Figure 14. Gate charge test circuit & waveforms

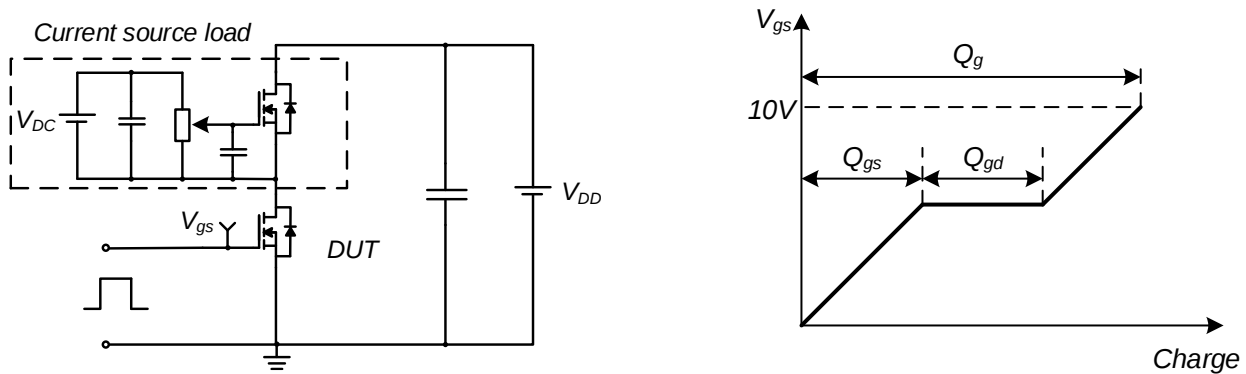


Figure 15. Switching time test circuit & waveforms

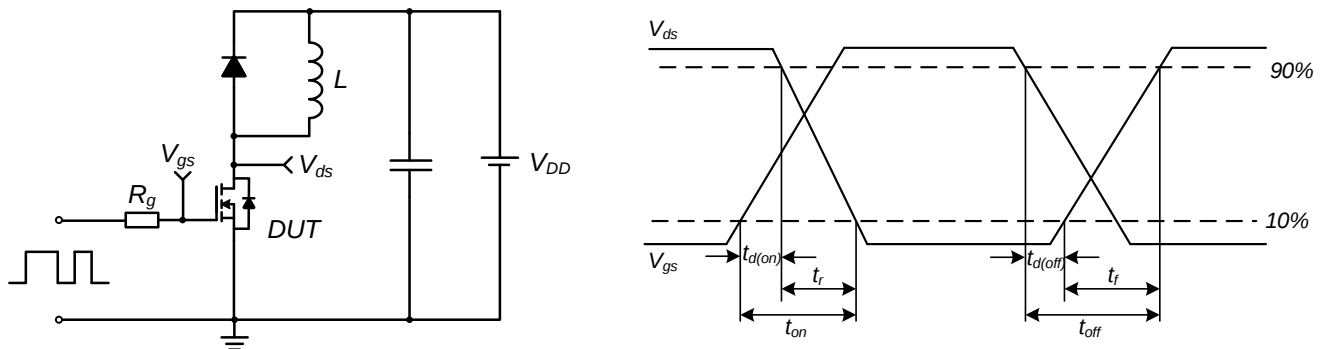


Figure 16. Diode reverse recovery test circuit & waveforms

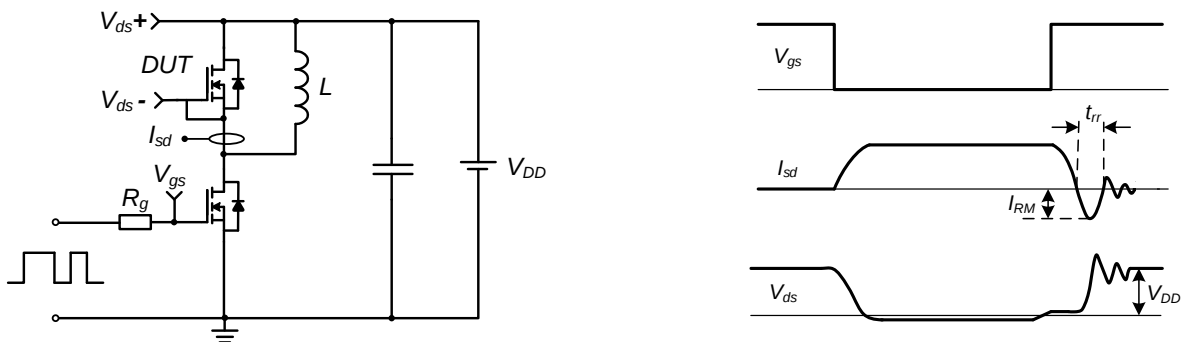
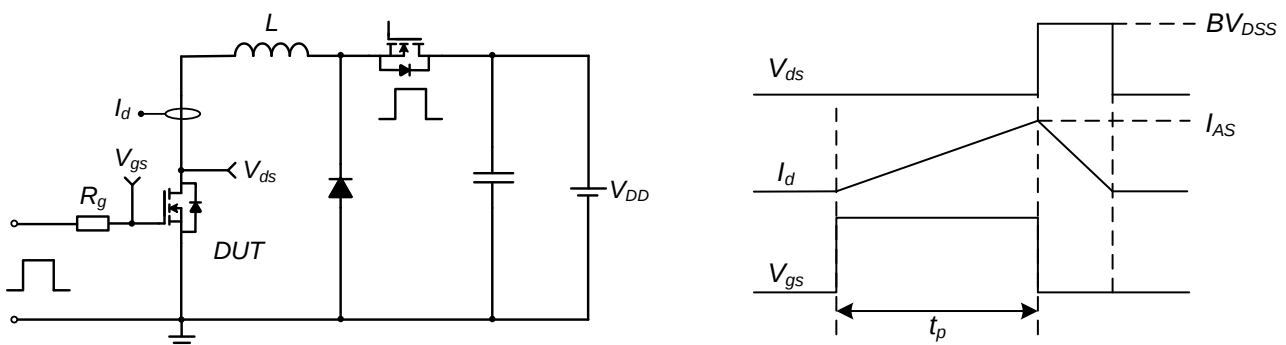
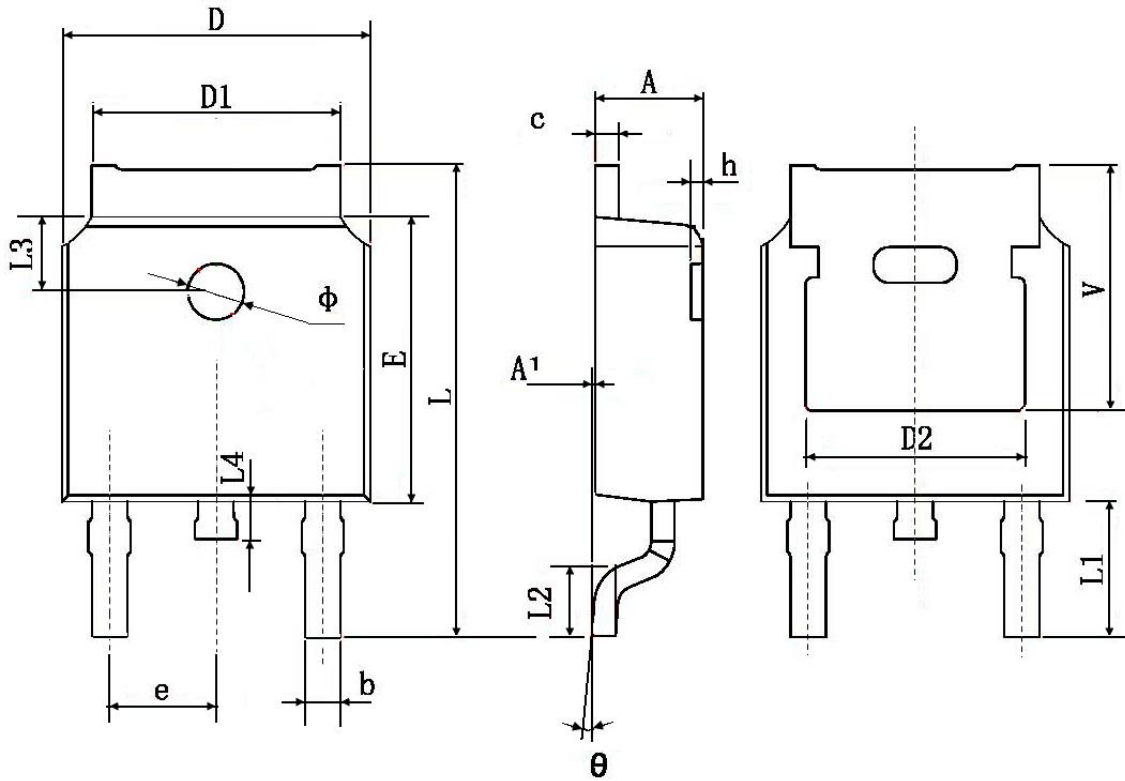


Figure 17. Unclamped inductive switching test circuit & waveforms



Package outline dimensions: TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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