GOSTONE

RoHS COMPLIANT

N-Channel 100V, 1.5mΩ max., TOLT MOSFET

GMS015N10M1

Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100	1.5 @ V_{GS} = 10V	480 (1)

General Information

Shipping

- One shipping options is offered as standard
- Un-sawn wafer

Handling

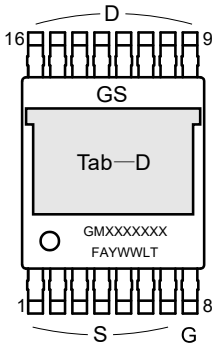
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environmen

Features

- Low RDS(on)
- Trench power MOSFET
- Low Gate Charge

Application

- Stored energy
- Electric motorcycle

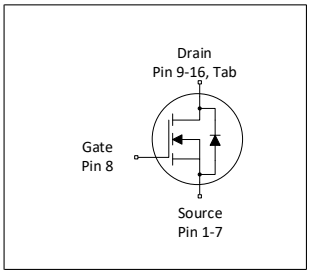


TOLT-16L

TOLT

NOTE:
LOGO - GS
GM - Part number code
F - Fab location code
A - Assembly location code
Y - Year code
WW - Week code
L&T - Assembly lot code

Equivalent circuit



Absolute Maximum Rating (Ta=25°C)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C=25℃ (1)	I_D	480	A
	T_C=100℃ (1)		336	
Pulsed drain current(2)		$I_{D,pulse}$	1920	
Avalanche energy, single pulse(3)		E_{AS}	1750	mJ
Power dissipation	T_C=25℃	P_D	517	W
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	℃

Thermal Characteristic (Ta=25°C)

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.29	℃/W
Thermal resistance, junction-to-ambient (4)	Steady state	$R_{\theta JA}$	40	

Electrical characteristics (Ta=25°C ± 3°C)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	100			V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 100 A		1.2	1.5	mΩ
Forward transconductance(5)	g_{fs}	V_{DS} = 5 V, I_D = 100 A		280		S
Gate resistance	R_g	f = 1 MHz, open drain		1.4	2	Ω
Dynamic(5)						
Total gate charge	Q_g	V_{DS} = 50 V, I_D = 100 A, V_{GS} = 10 V		258	362	nC
Gate-source charge	Q_{gs}			68	96	
Gate-drain charge	Q_{gd}			74	104	
Turn-on delay time	$t_{d(on)}$	V_{DS} = 50 V, I_D = 100 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		64	128	ns
Rise time	t_r			61	122	
Turn-off delay time	$t_{d(off)}$			221	442	
Fall time	t_f			104	208	
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		15650	21910	pF
Output capacitance	C_{oss}			2100	2940	
Reverse transfer capacitance	C_{rss}			45	90	
Reverse Diode Characteristics(5)						
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 100 A		0.8	1.1	V
Reverse recovery time	t_{rr}	V_{DS} = 50 V,I_F = 100 A, di/dt = 100 A/μs		126	227	ns
Reverse recovery charge	Q_{rr}			427	769	nC

Notes

(1) Package limited.
(2) Pulse width limited by maximum junction temperature.
(3) V_{DS} = 75 V, V_{GS} = 10 V, L = 0.3 mH.
(4) $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
(5) Guaranteed by design, not subject to production testing.

Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

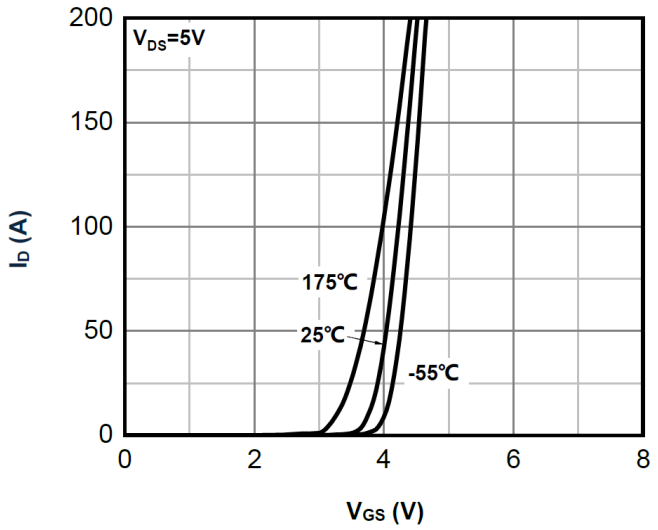


Fig.2 Typ. output characteristics

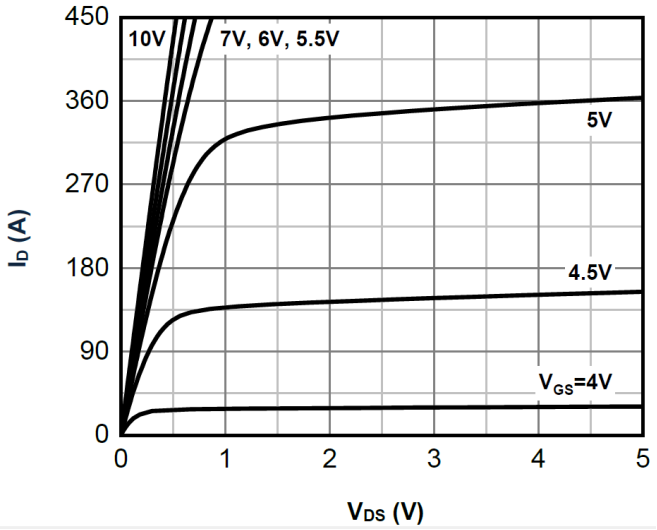


Fig.3 Normalized on-resistance vs drain current

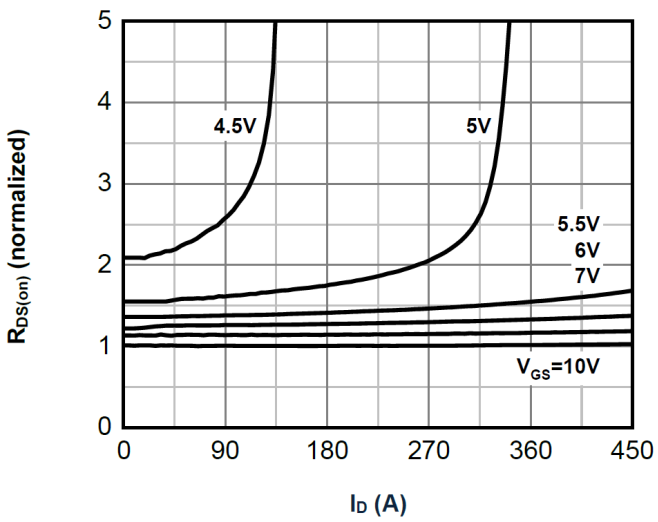


Fig.4 Typ. on-resistance vs gate-source voltage

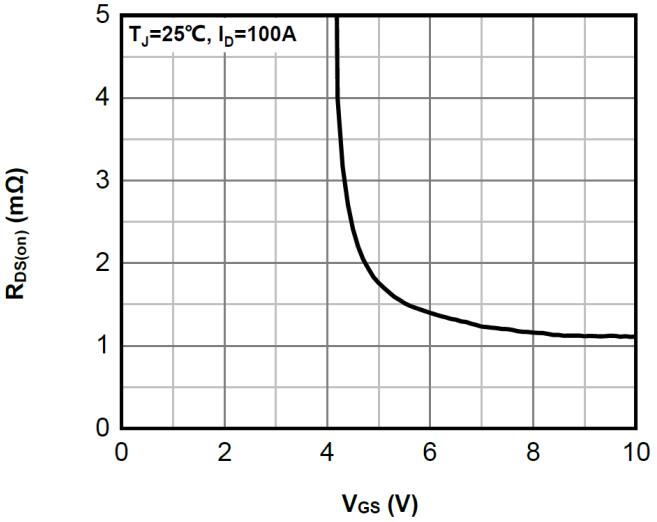


Fig.5 Normalized on-resistance vs junction temperature

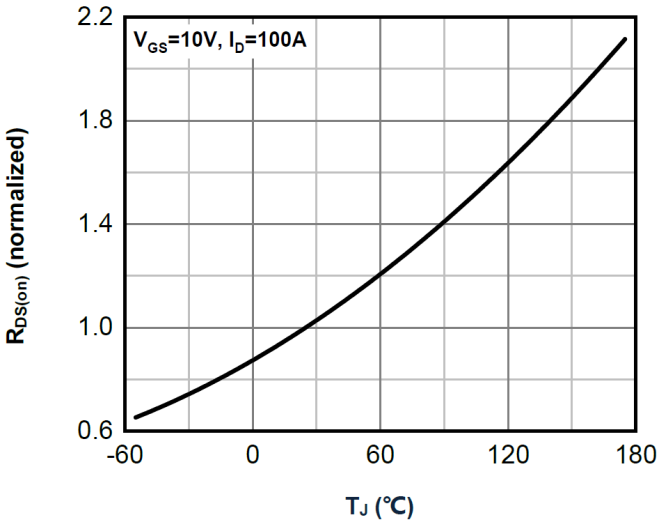


Fig.6 Typ. gate charge

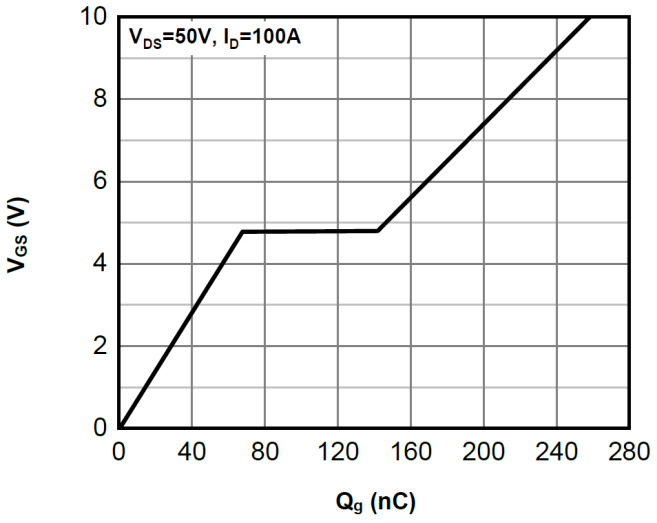


Fig.7 Typ. forward characteristics of body diode

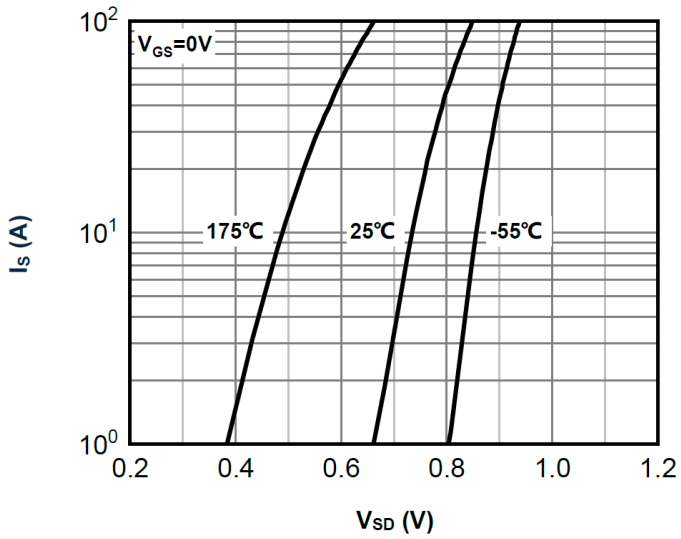


Fig.8 Safe operating area

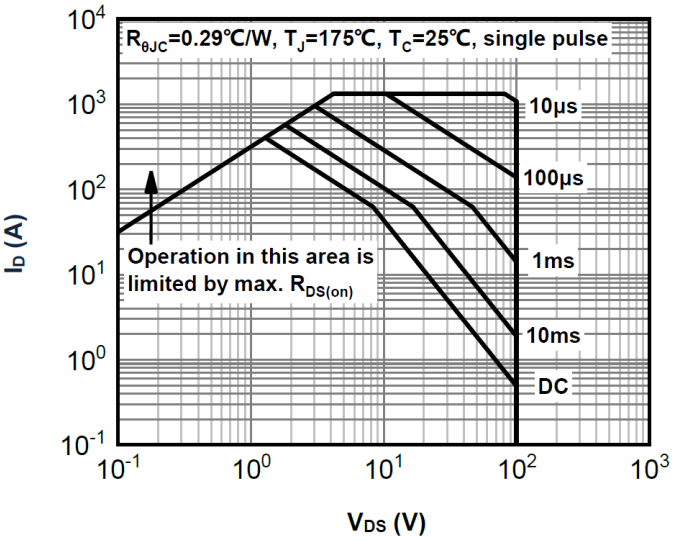


Fig.12 Max. continuous drain current vs case temperature

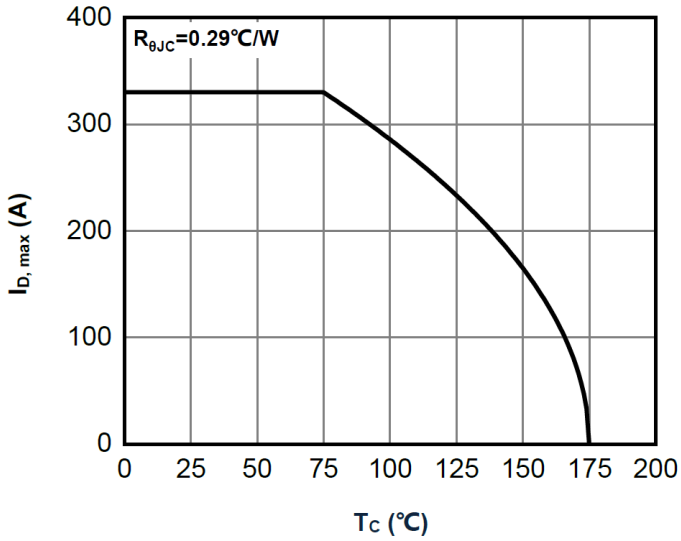


Fig.10 Single pulse maximum power dissipation

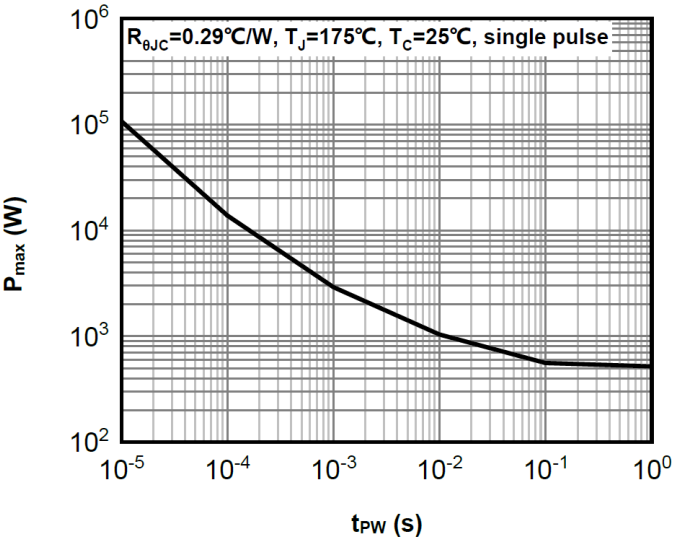


Fig.11 Max. power dissipation vs case temperature

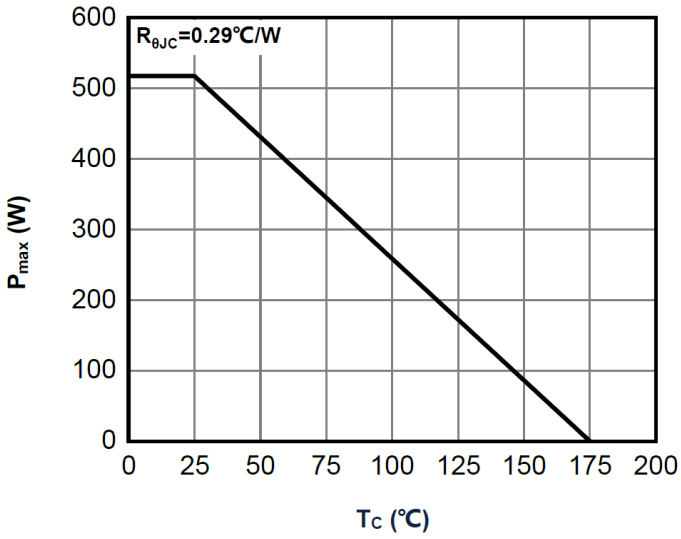


Fig.9 Typ. Capacitance

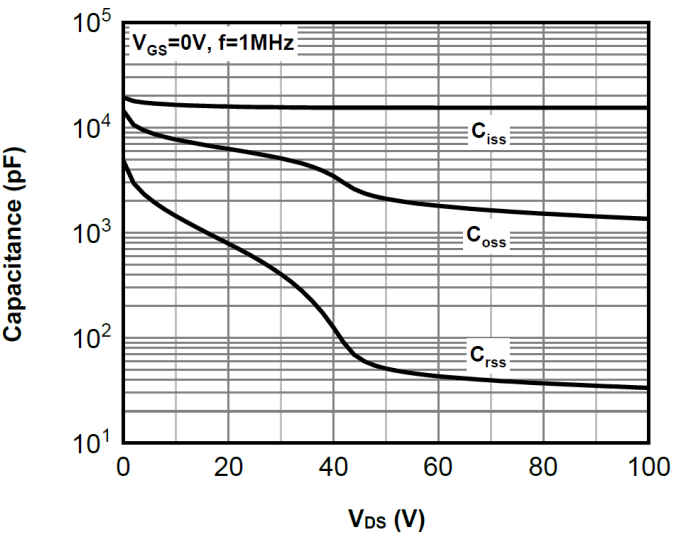


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

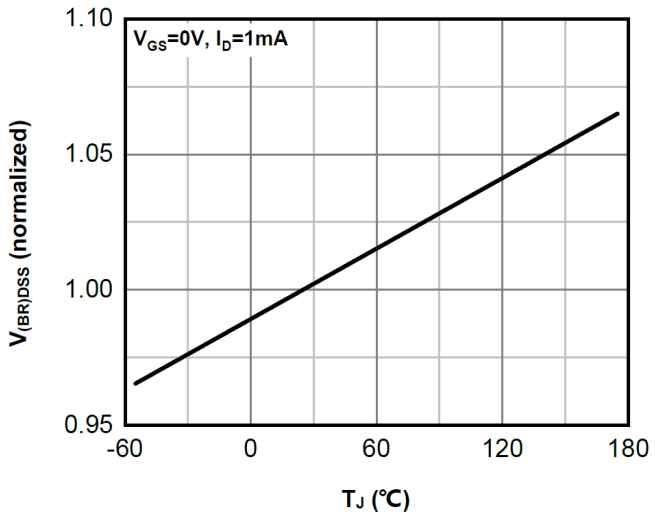


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

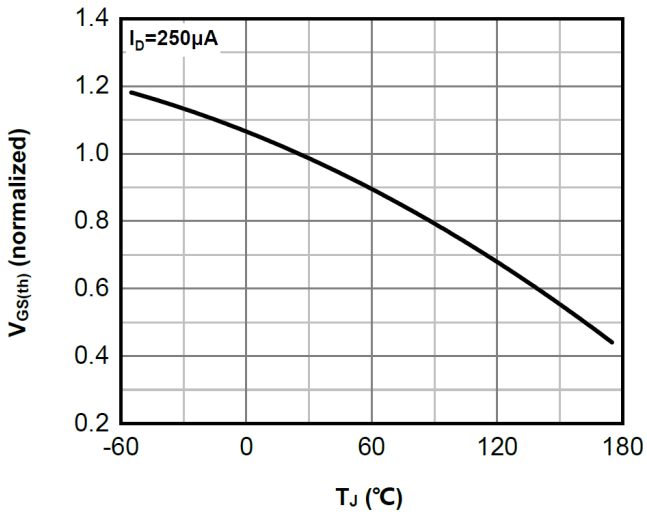
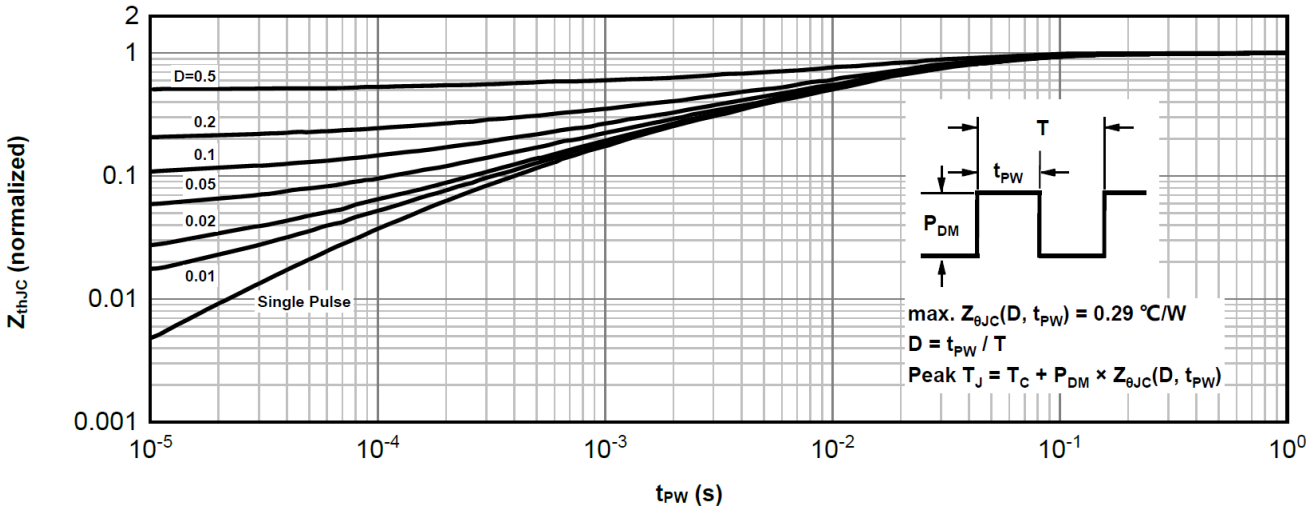
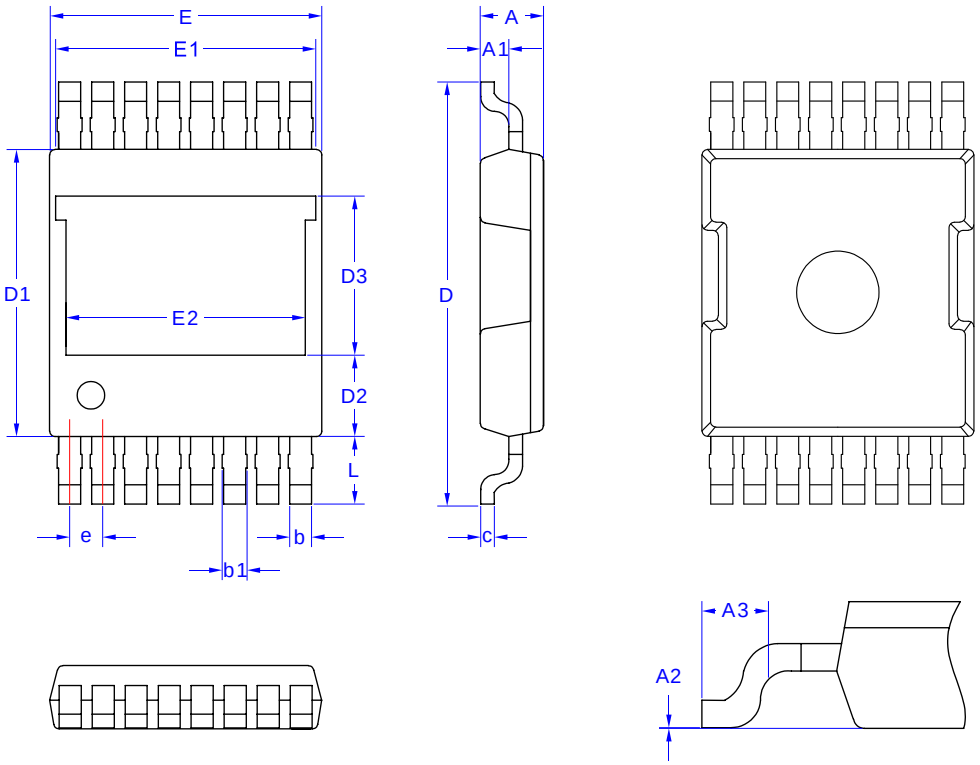


Fig.15 Normalized transient thermal impedance from junction to case



Package outline dimensions: TOLT



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.99	1.04	1.09
A2	0.00	0.08	0.16
A3	1.50 REF		
b	0.70	0.75	0.80
b1	0.65	0.70	0.75
c	0.45	0.50	0.55
D	14.50	15.00	15.50

Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
D1	9.60	10.10	10.60
D2	2.30	2.80	3.30
D3	5.77 REF		
E	9.40	9.90	10.40
E1	9.46 REF		
E2	8.70 REF		
e	1.15	1.20	1.25
L	2.40	2.45	2.50

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