

Product Summary

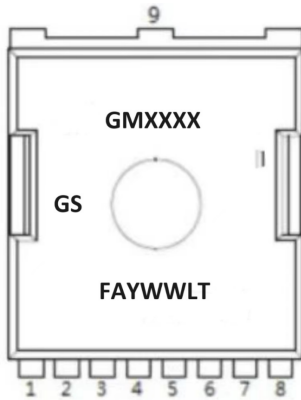
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
60	1.6 @ $V_{GS} = 10V$	300 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- DC/DC conversion
- Power switch
- Motor drives



TOLL

NOTE:
 LOGO - GS
 GMXXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

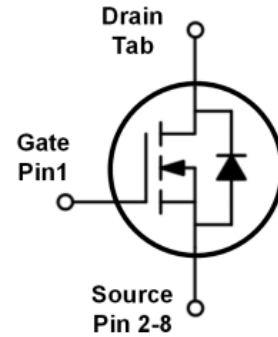
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	60	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C ⁽¹⁾	I _D	300	A
	T _C =100°C		220	
	T _A =25°C ⁽⁴⁾		31	
Pulsed drain current ⁽²⁾		I _{D,pulse}	1100	
Avalanche energy, single pulse ⁽³⁾		E _{AS}	625	mJ
Power dissipation	T _C =25°C	P _D	300	W
	T _A =25°C ⁽⁴⁾		2.9	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to 150	°C

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	43	

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	60			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.7	2.5	3.3	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 100 A		1.2	1.6	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 100 A		121		S
Gate resistance	R _g	f = 1 MHz		2		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 30 V, I _D = 30 A, V _{GS} = 10 V		142		nC
Gate-source charge	Q _{gs}			28		
Gate-drain charge	Q _{gd}			47		
Turn-on delay time	t _{d(on)}	V _{DS} = 30 V, I _D = 100 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		16		ns
Rise time	t _r			88		
Turn-off delay time	t _{d(off)}			36		
Fall time	t _f			26		
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		7450		pF
Output capacitance	C _{oss}			1680		
Reverse transfer capacitance	C _{rss}			90		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 100 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 30 V, I _F = 50 A, di/dt = 100 A/μs		79		ns
Reverse recovery charge	Q _{rr}			180		nC

Notes

- (1) Limited by maximum junction temperature..
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 0.5\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

Electrical characteristics diagrams

Typical Characteristics

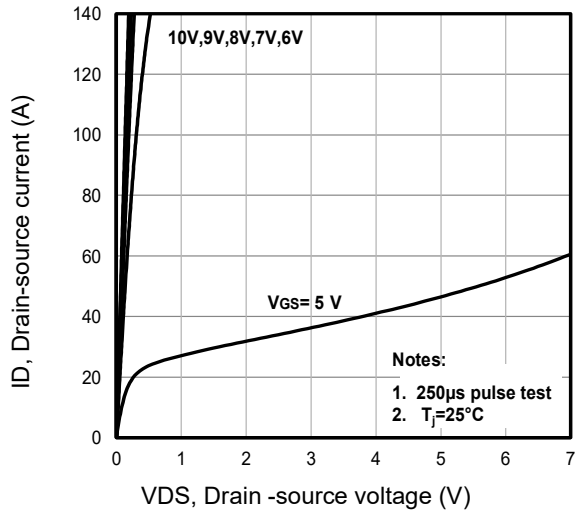


Fig1. Typical output characteristics

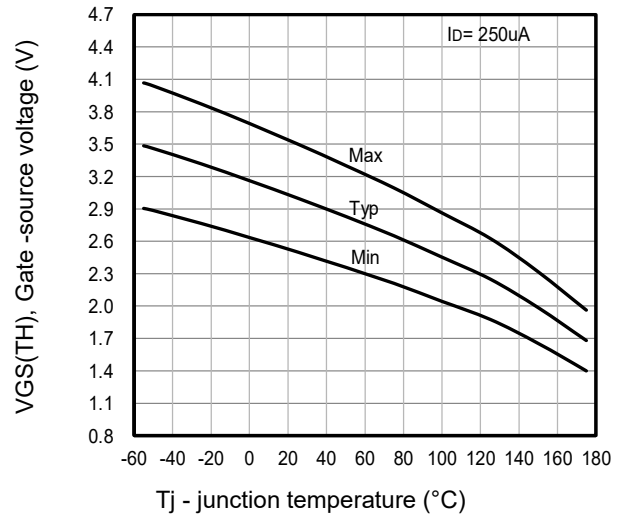


Fig2. Typical $V_{GS(TH)}$ gate-source voltage Vs. T_j

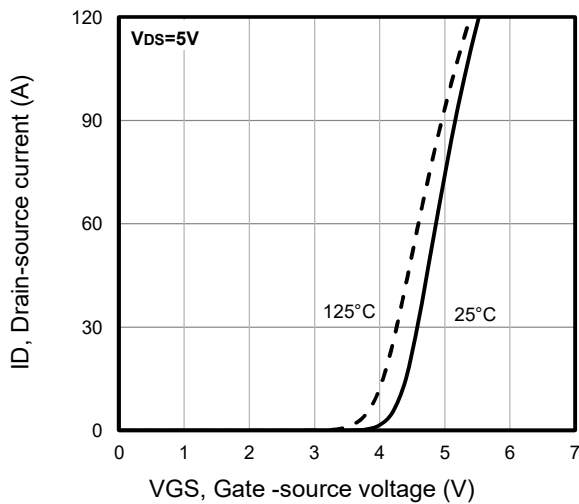


Fig3. Typical transfer characteristics

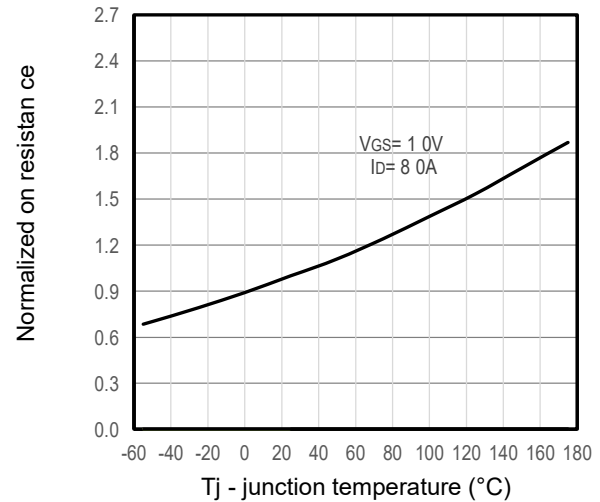


Fig4. Typical normalized on-resistance Vs. T_j

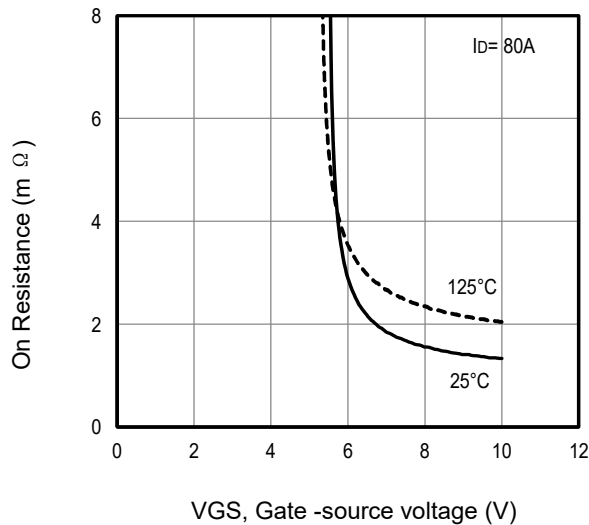


Fig5. Typical on resistance Vs gate-source voltage

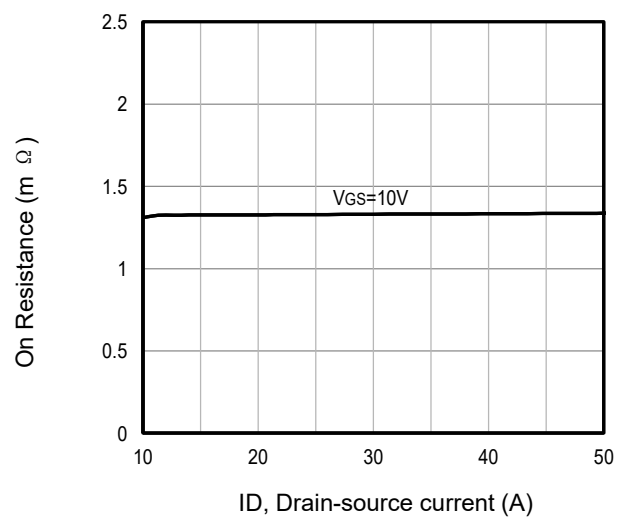


Fig6. Typical on resistance Vs drain current

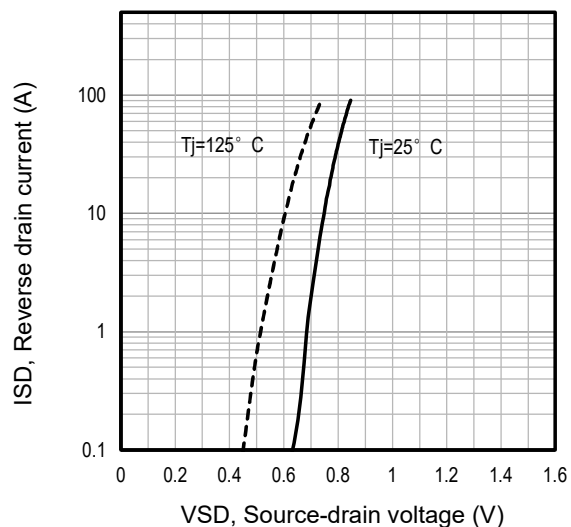


Fig7. Typical source-drain diode forward voltage

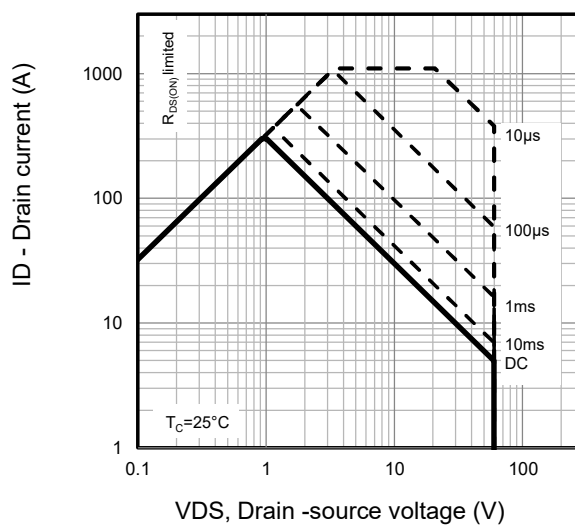


Fig8. Maximum safe operating area

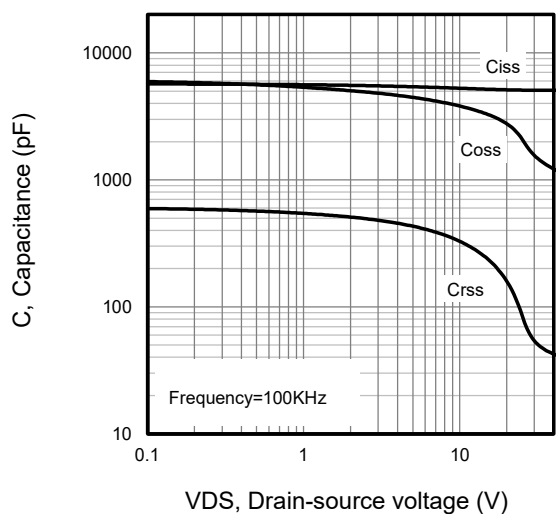


Fig9. Typical capacitance Vs. drain-source voltage

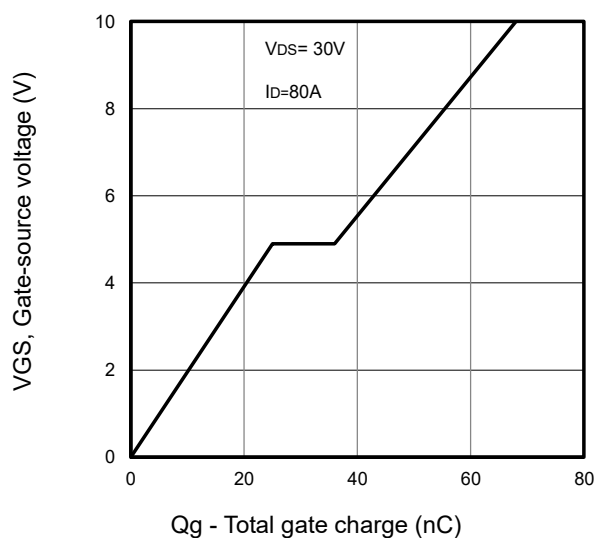


Fig10. Typical gate charge Vs. gate-source voltage

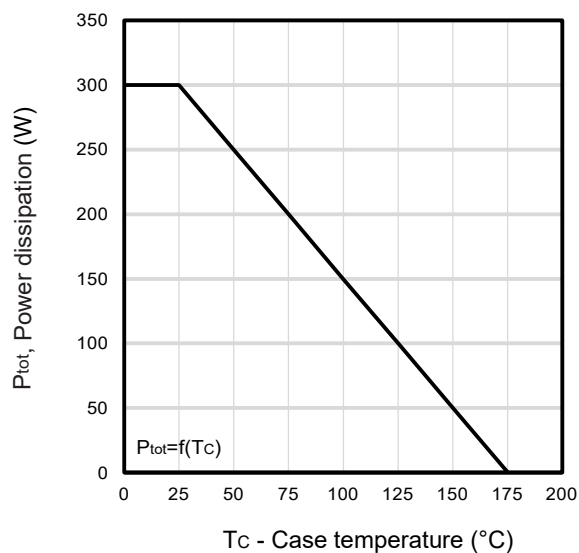


Fig11. Power dissipation Vs. case temperature

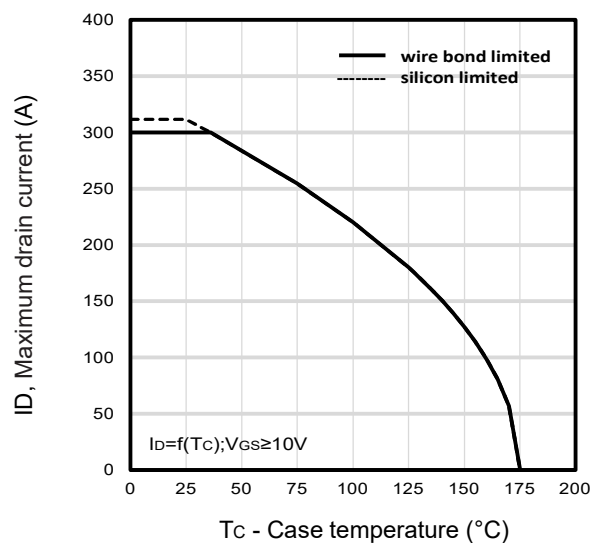


Fig12. Maximum drain current Vs. case temperature

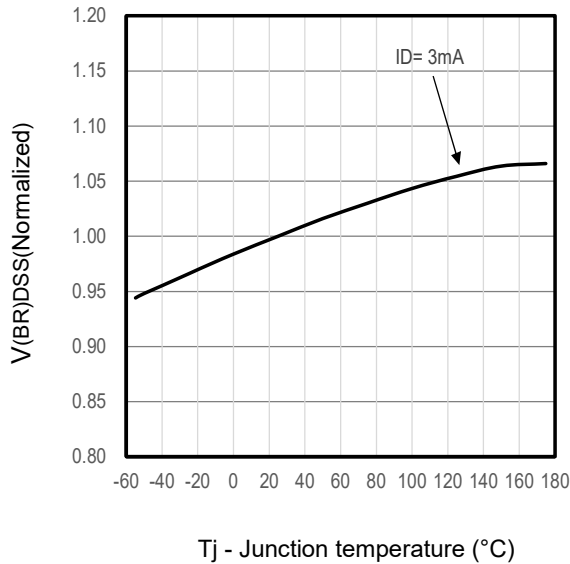


Fig13. Typical $V(BR)DSS$ Vs T_j

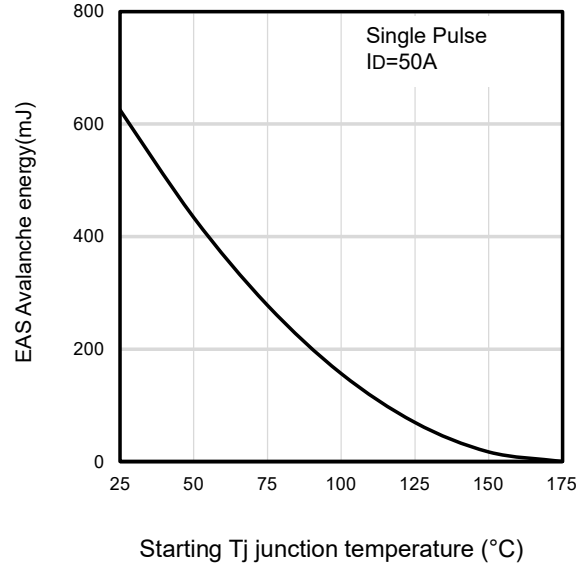


Fig14. Maximum avalanche energy vs temperature ($^{\circ}C$)

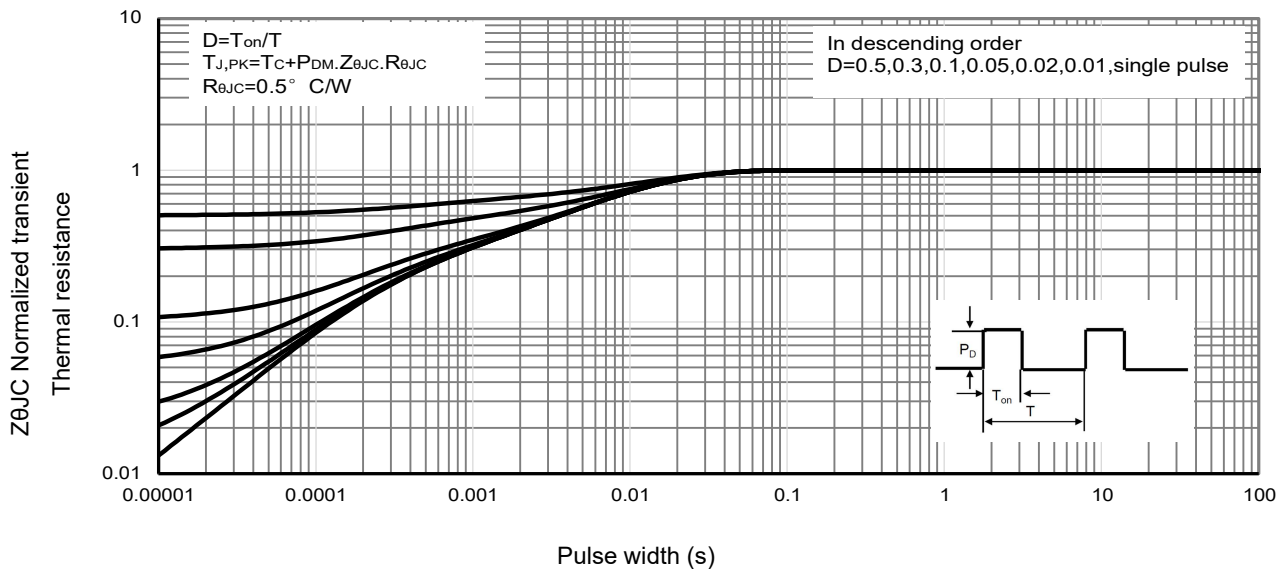


Fig15. Normalized maximum transient thermal impedance

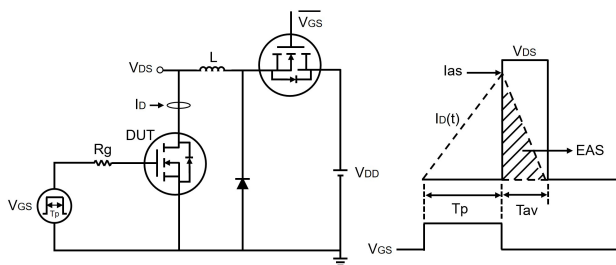


Fig16. Unclamped inductive test circuit and waveforms

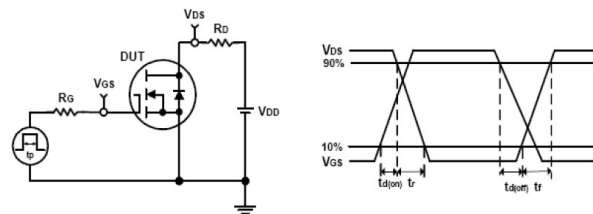
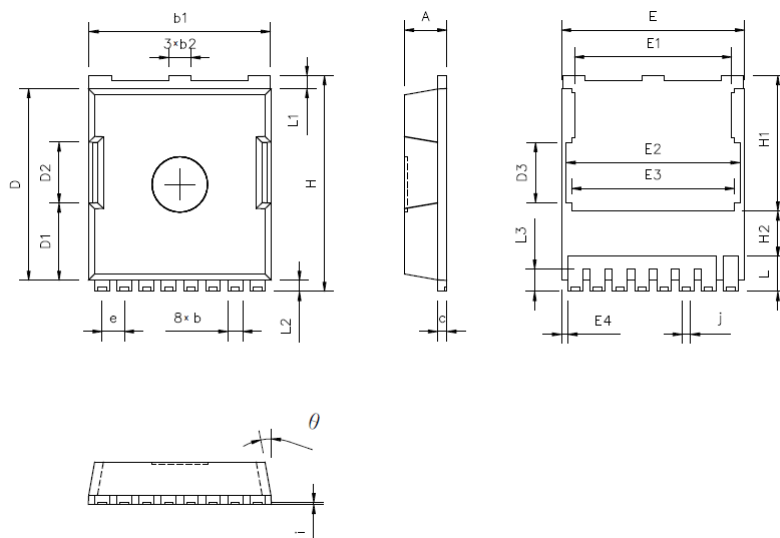


Fig17. Switching time test circuit and waveforms

Package outline dimensions: TOLL


Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
ø	10° REF		

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