

Product Summary

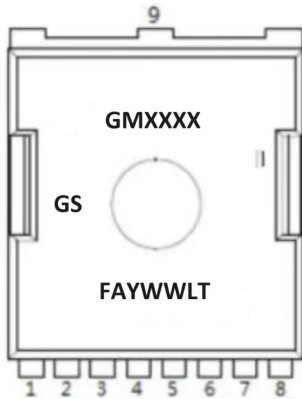
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
150	3.0 @ $V_{GS} = 10V$	250 ⁽¹⁾

Features

- ❖ Low $R_{DS(on)}$
- ❖ Trench power MOSFET
- ❖ Low Gate Charge

Application

- ❖ Stored energy
- ❖ Electric motorcycle
- ❖ DC/DC Converter
- ❖ Synchronous Rectification in SMPS
- ❖ Hard Switching and High Speed Circuit



TOLL

NOTE:
 LOGO - GS
 GMXXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

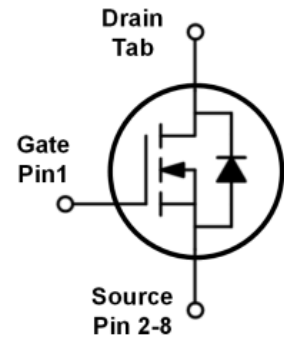
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	150	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	$T_C=25^\circ\text{C}$ ⁽¹⁾	I_D	A
	$T_C=100^\circ\text{C}$	250	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	850	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	2025	mJ
Power dissipation	$T_C=25^\circ\text{C}$	P_D	265 W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.47	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	40	

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	150			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.1	3.2	4.1	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 150 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		2.85	3.0	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 20 A		53		S
Gate resistance	R _g	f = 1 MHz, open drain		2.6		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 75 V, I _D = 40 A, V _{GS} = 10 V		150		nC
Gate-source charge	Q _{gs}			56		
Gate-drain charge	Q _{gd}			30		
Turn-on delay time	t _{d(on)}	V _{DS} = 75 V, I _D = 40 A, V _{GS} = 10 V, R _{GEN} = 3 Ω		41		ns
Rise time	t _r			67		
Turn-off delay time	t _{d(off)}			85		
Fall time	t _f			34		
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		9860		pF
Output capacitance	C _{oss}			2054		
Reverse transfer capacitance	C _{rss}			21		
Reverse Diode Characteristics(5)						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 100 A		0.7	1.2	V
Reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs		99		ns
Reverse recovery charge	Q _{rr}			320		nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 1\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

Electrical characteristics diagrams

Fig 1: Output Characteristics

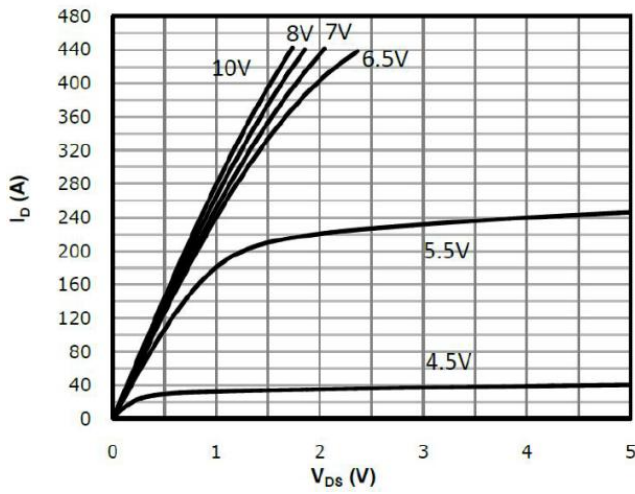


Fig 2: Transfer Characteristics

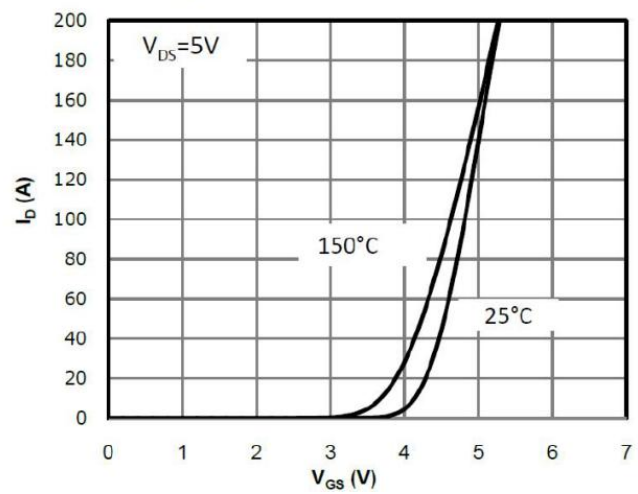


Fig 3: Rds(on) vs Drain Current and Gate Voltage

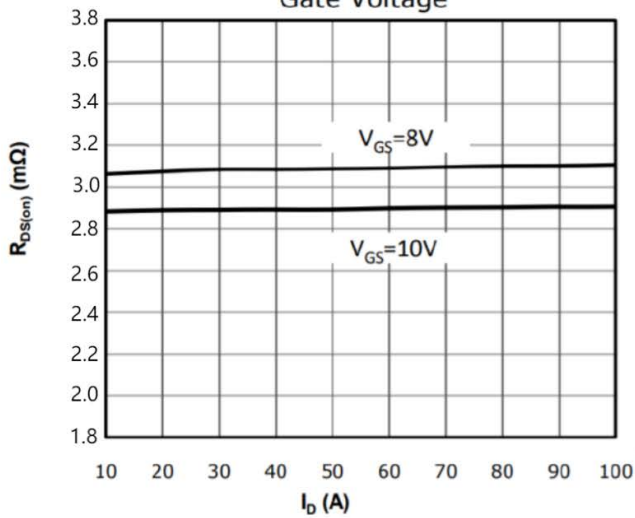


Fig 4: Rds(on) vs Gate Voltage

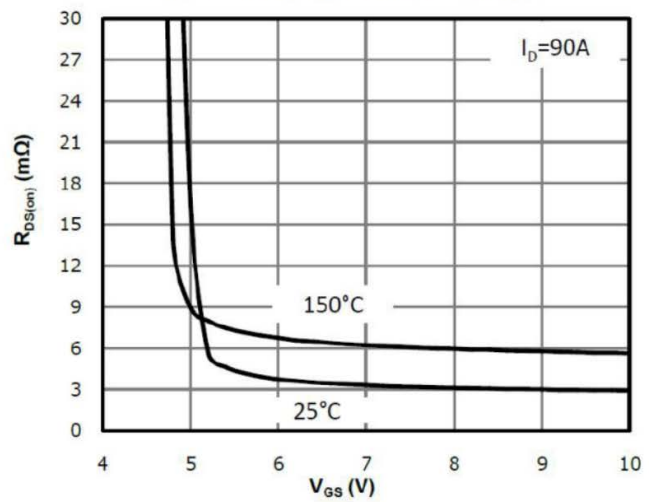


Fig 5: Rds(on) vs. Temperature

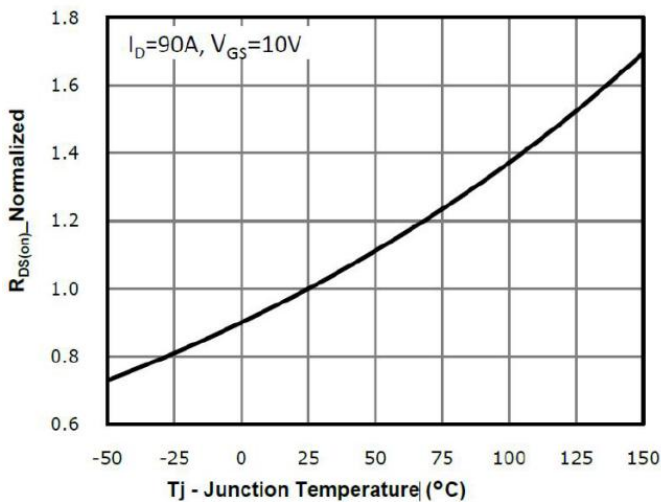
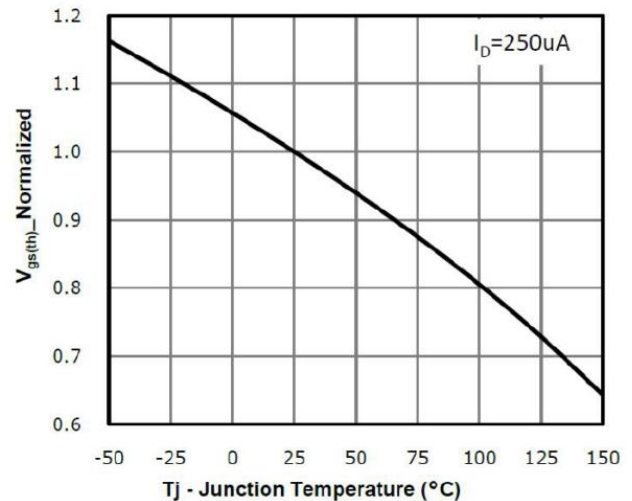


Fig 6: Vgs(th) vs. Temperature



Electrical characteristics diagrams

Fig 7: BVdss vs. Temperature

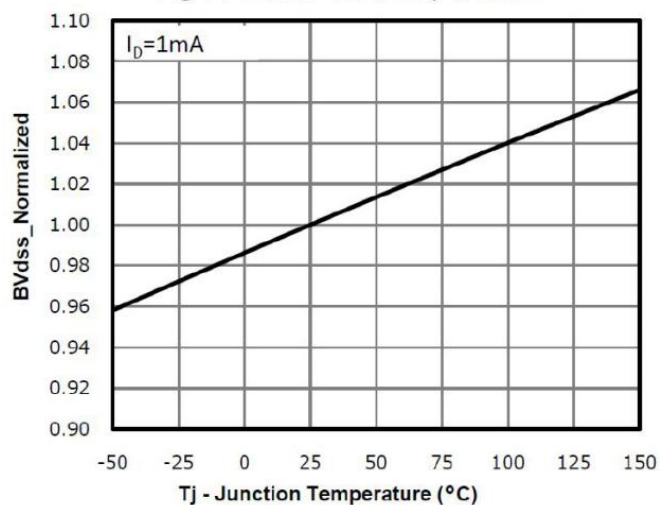


Fig 8: Capacitance Characteristics

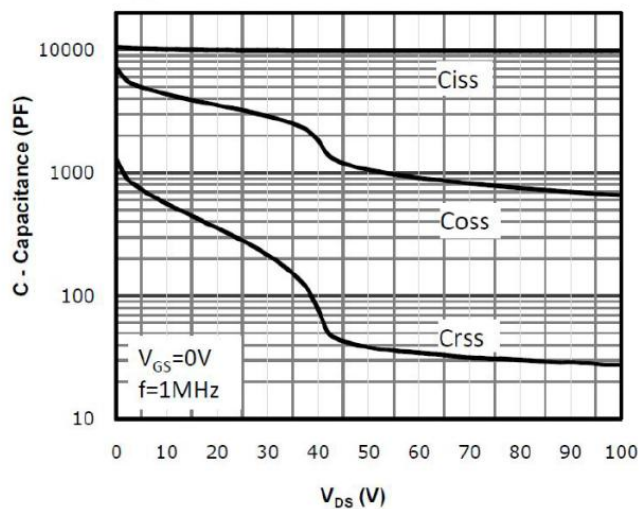


Fig 9: Gate Charge Characteristics

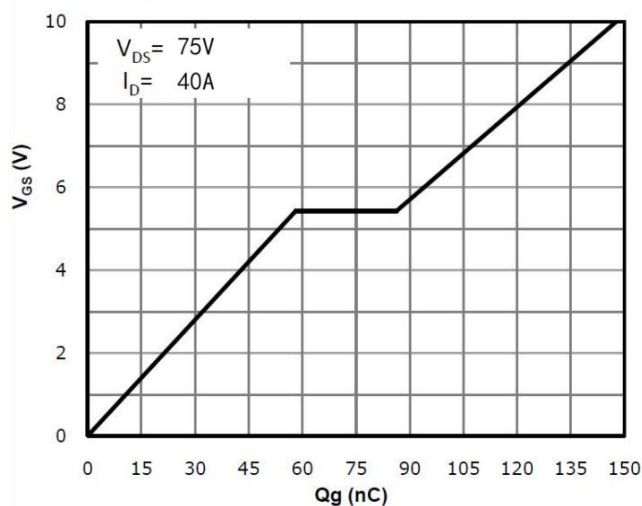


Fig 10: Body-diode Forward Characteristics

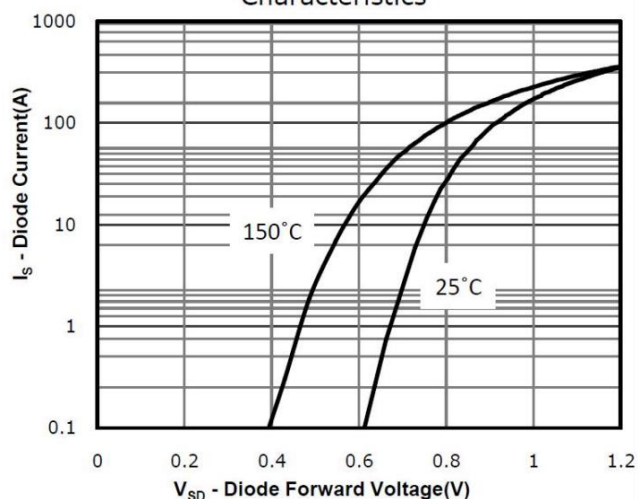


Fig 11: Power Dissipation

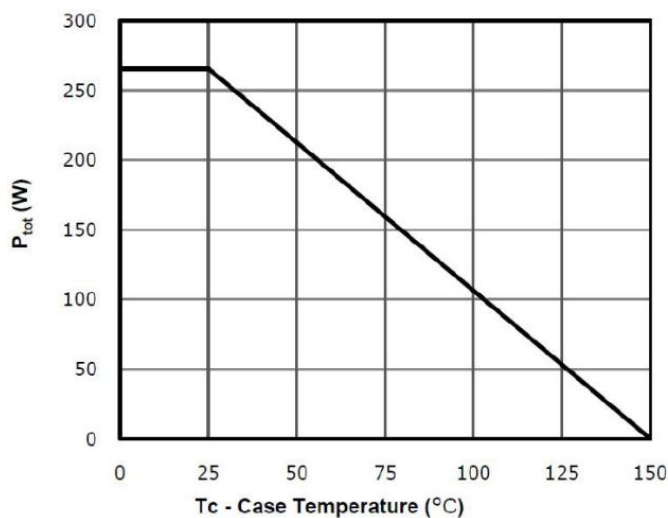
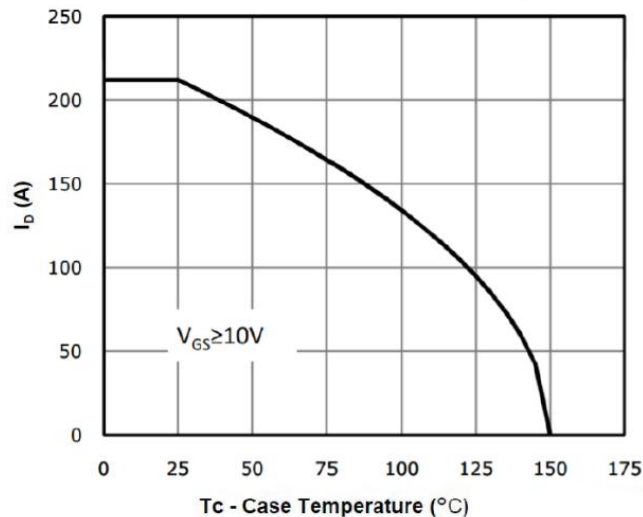


Fig 12: Drain Current Derating



Electrical characteristics diagrams

Fig 13: Safe Operating Area

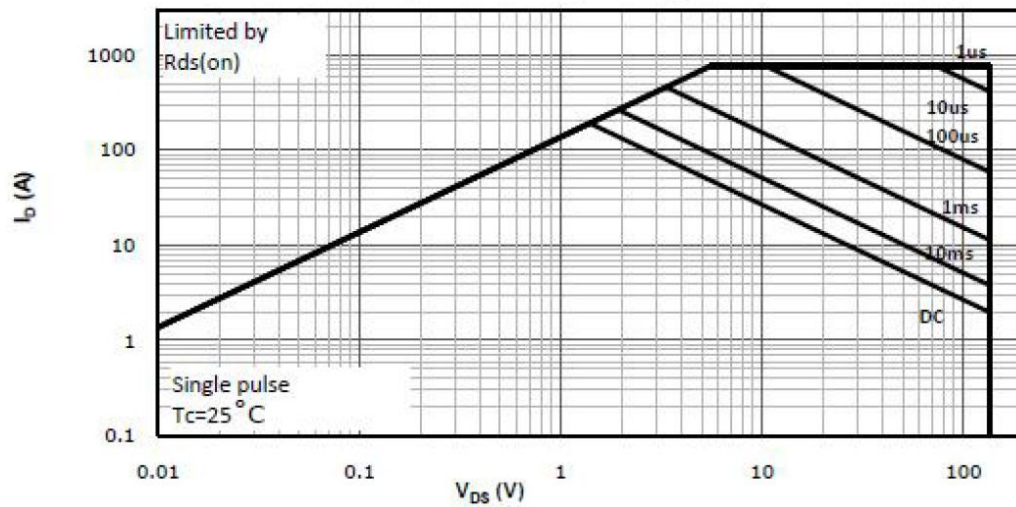
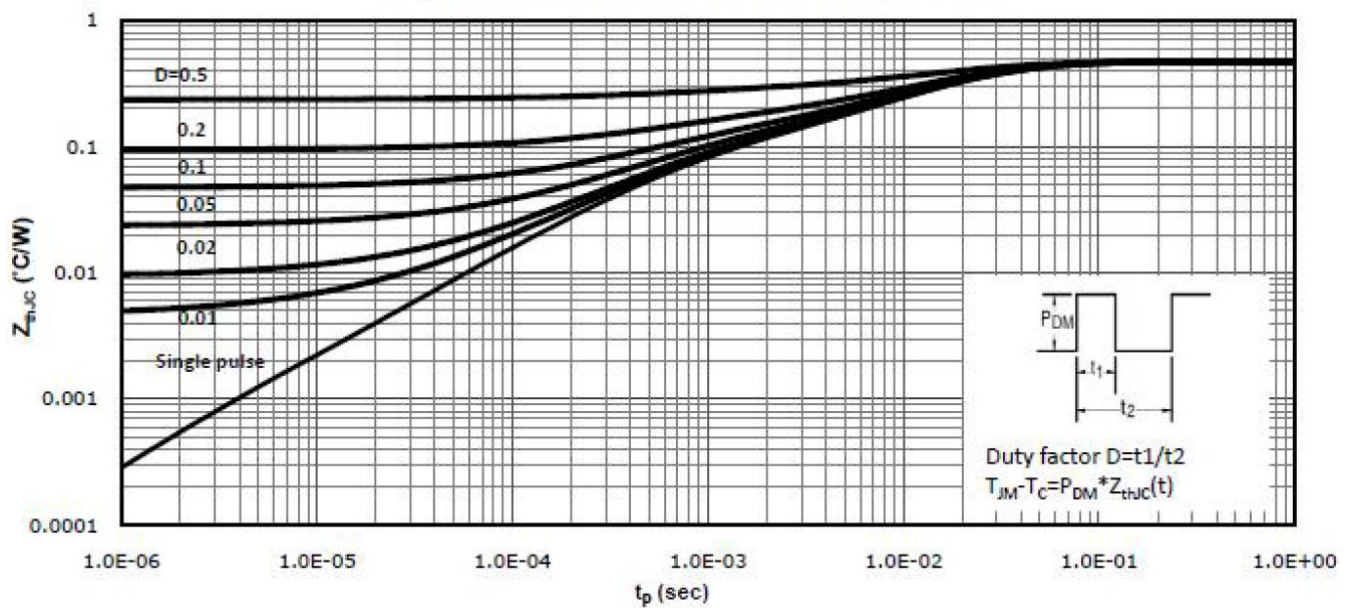
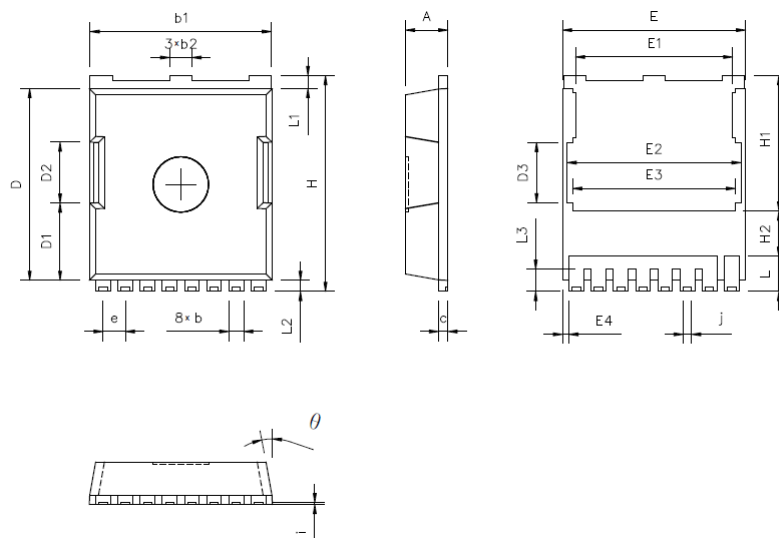


Fig 14: Max. Transient Thermal Impedance



Package outline dimensions: TOLL


Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
θ	10° REF		

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