

Product Summary

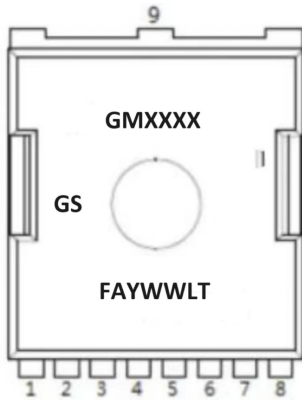
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
200	10.0 @ $V_{GS} = 10V$	110 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- DC/DC conversion
- Power switch
- Synchronous Rectification in SMPS



TOLL

NOTE:
 LOGO - GS
 GMXXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

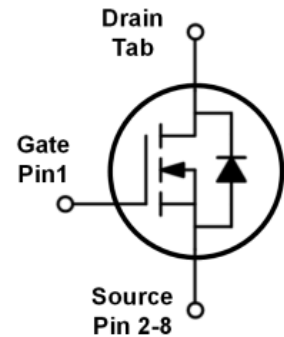
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	200	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	110	A
		78	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	440	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	1440	mJ
Power dissipation	P_D	333	W
		167	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Electrical characteristics (Ta=25°C ± 3°C)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	200			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5	3.4	4.5	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 100\text{ A}$		8.6	10	m Ω
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5\text{ V}$, $I_D = 100\text{ A}$		50		S
Gate resistance	R_g	$f = 1\text{ MHz}$		3.0		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 100\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$		45		nC
Gate-source charge	Q_{gs}			30		
Gate-drain charge	Q_{gd}			13		
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 100\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 3\text{ }\Omega$		13		ns
Rise time	t_r			29		
Turn-off delay time	$t_{d(off)}$			37		
Fall time	t_f			31		
Input capacitance	C_{iss}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2996		pF
Output capacitance	C_{oss}			462		
Reverse transfer capacitance	C_{rss}			13		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}$, $I_F = 2.0\text{ A}$		0.7	1.2	V
Reverse recovery time	t_{rr}	$I_F = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		124		ns
Reverse recovery charge	Q_{rr}			644		nC

Notes

- (1) Limited by maximum junction temperature..
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, L = 1.0\text{ mH}$.
- (4) Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
- (5) Guaranteed by design, not subject to production testing.

Thermal Characteristic (Ta=25°C)

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.35	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	31	

Electrical characteristics diagrams

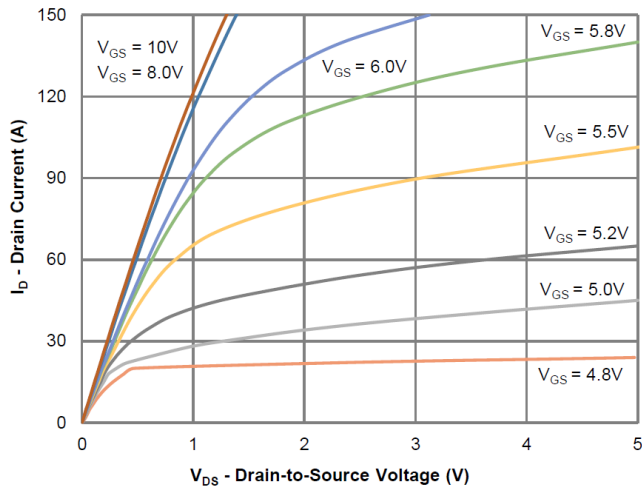


Figure 1: Output Characteristics

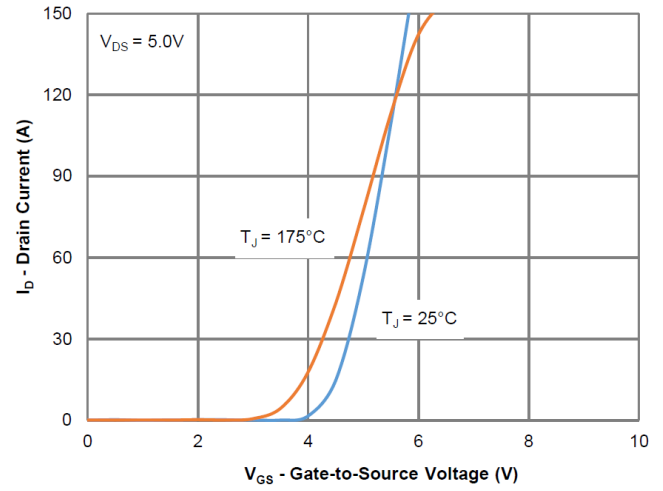


Figure 2: Transfer Characteristics

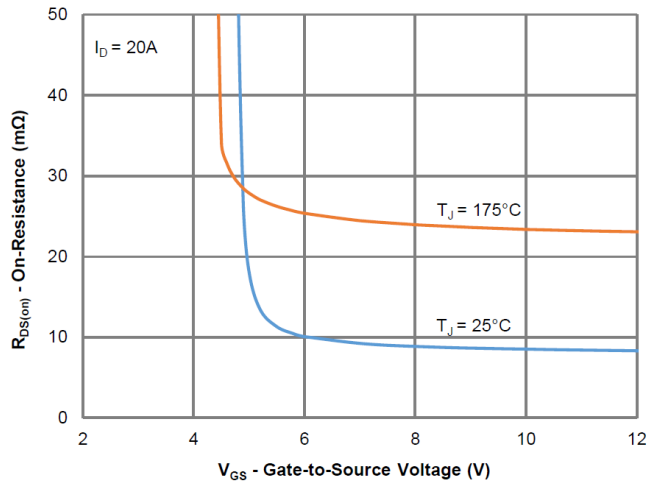


Figure 3: On-Resistance vs. Gate-Source Voltage

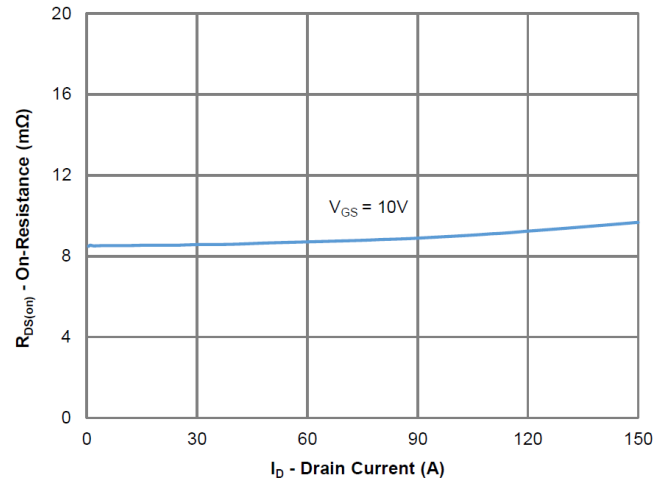


Figure 4: On-Resistance vs. Gate-Source Voltage

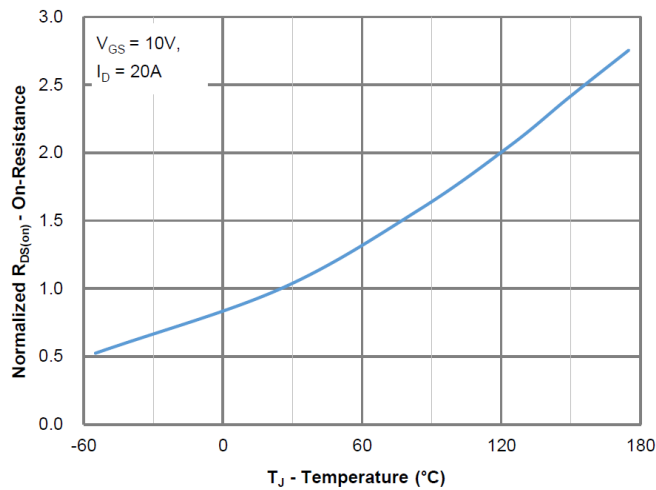


Figure 5: On-Resistance vs. Junction Temperature

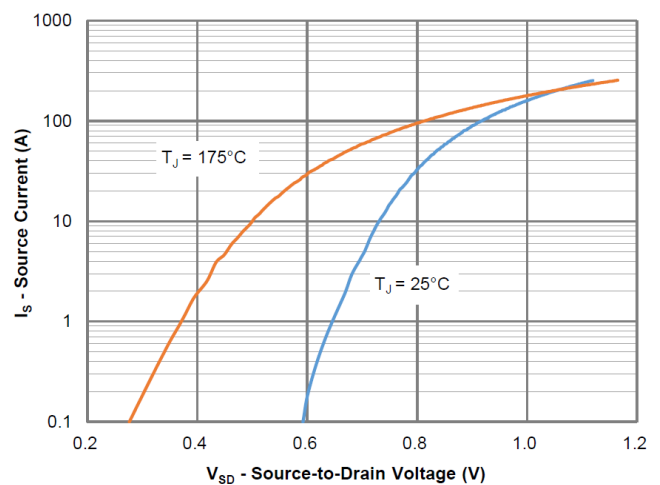


Figure 6: Source-Drain Diode Forward Voltage

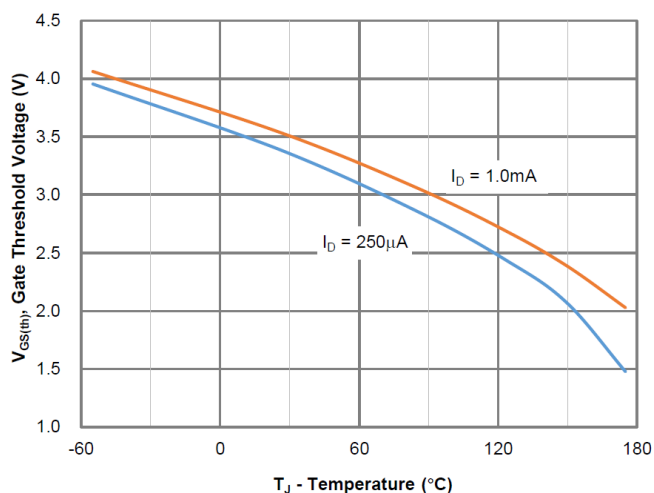


Figure 7: Gate Threshold Variation vs. Junction Temperature

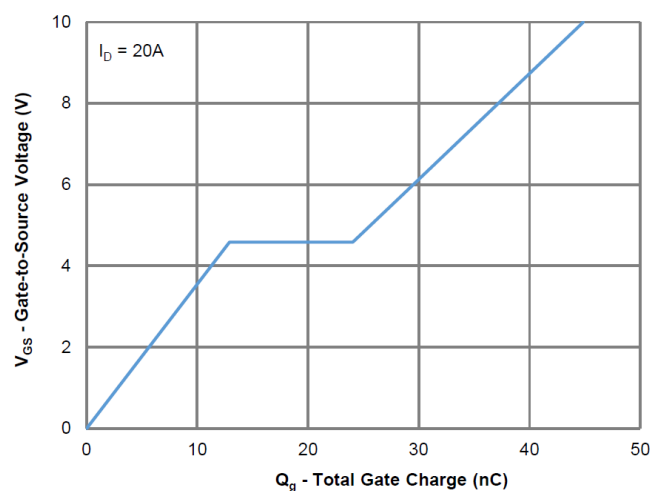


Figure 8: Gate Charge Characteristics

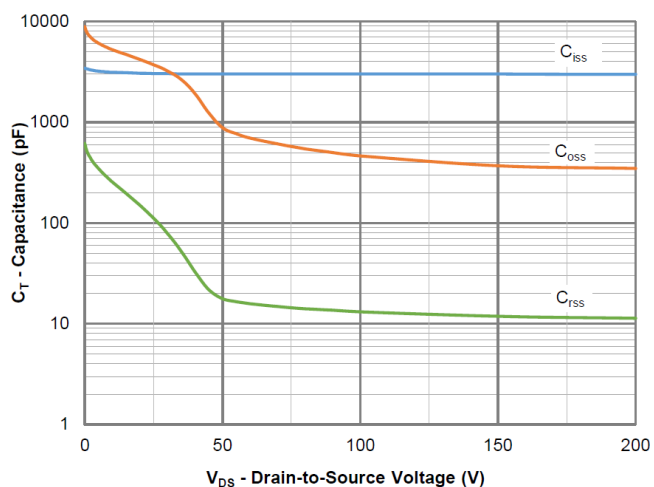


Figure 9: Capacitance Characteristics

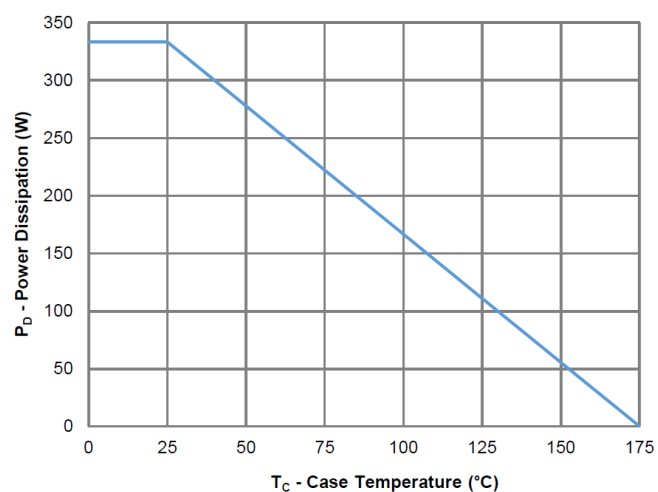


Figure 10: Power Derating

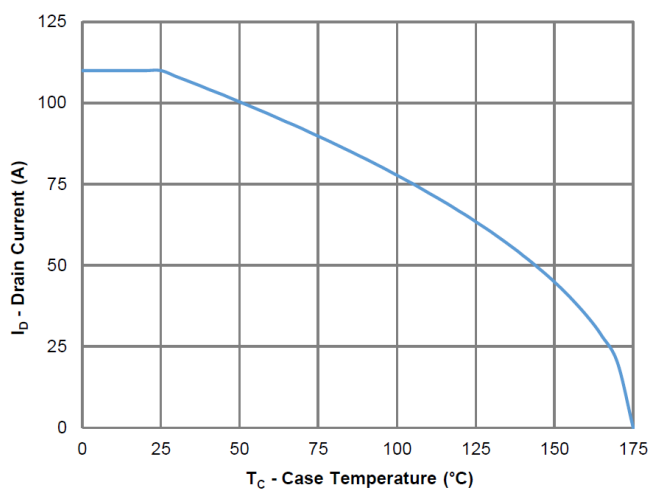


Figure 11: Current Derating

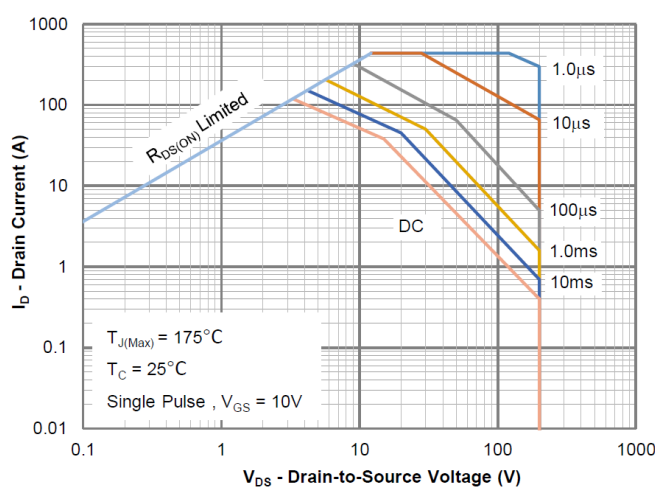


Figure 12: Safe Operating Area

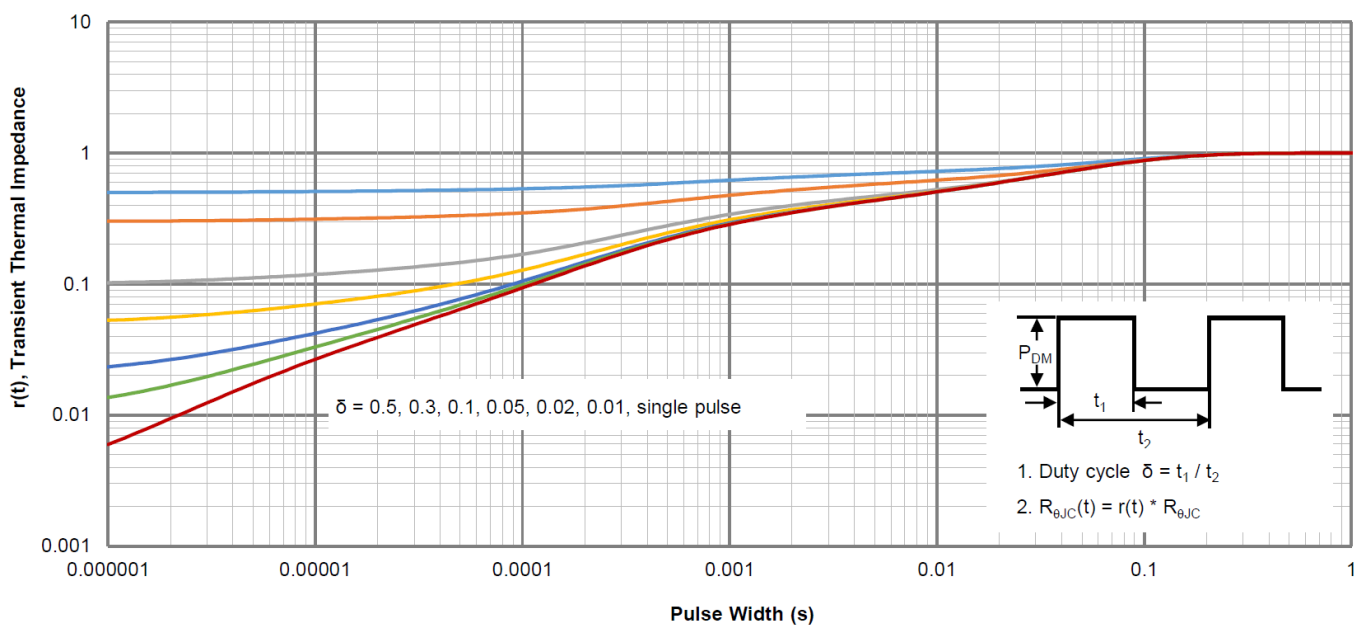
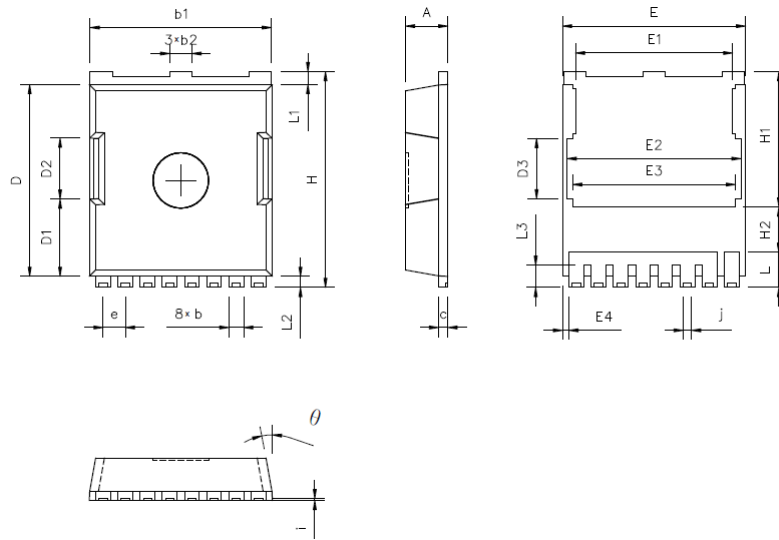


Figure 13: Normalized Maximum Transient Thermal Impedance

Package outline dimensions: TOLL


Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
θ	10° REF		

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