

Product Summary

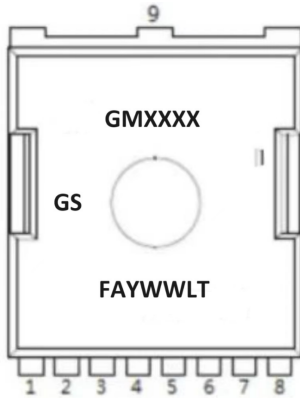
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
200	22 @ $V_{GS} = 10V$	61 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- DC/DC conversion
- Power switch
- Synchronous Rectification in SMPS



TOLL

NOTE:
 LOGO - GS
 GMXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

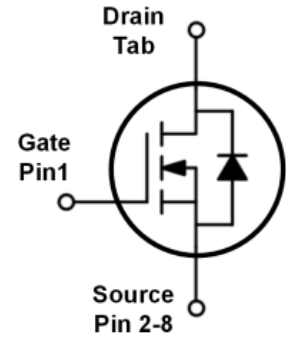
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environment

Equivalent circuit



Absolute maximum rating@25°C

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	200	V
Gate-source voltage	V_{GS}	±20	
Continuous drain current	I_D	61	A
	I_D	43	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	244	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	542	mJ
Power dissipation	P_D	254	W
	P_D	127	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	°C

Thermal Characteristic

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.59	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	35	

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0, I _D = 250 μA	200			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5	3.4	4.5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		20.6	22	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 20 A		40		S
Gate resistance	R _g	f = 1 MHz		2.5		Ω
Dynamic ⁽⁵⁾						
Total gate charge V _{GS} = 10 V	Q _g	V _{DS} = 100 V, I _D = 20 A, V _{GS} = 10 V		35		nC
Gate-source charge	Q _{gs}			11.5		
Gate-drain charge	Q _{gd}			7.5		
Turn-on delay time	t _{d(on)}	V _{DS} = 100 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 3 Ω		8.6		ns
Rise time	t _r			17		
Turn-off delay time	t _{d(off)}			28		
Fall time	t _f			22		
Input capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		2363		pF
Output capacitance	C _{oss}			184		
Reverse transfer capacitance	C _{rss}			12.1		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 2 A		0.7	1.2	V
Reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs		100		ns
Reverse recovery charge	Q _{rr}			419		nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 100 V, V_{GS} = 10 V, L = 1.0 mH$.
- (4) Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
- (5) Guaranteed by design, not subject to production testing.



Typical Performance Characteristics

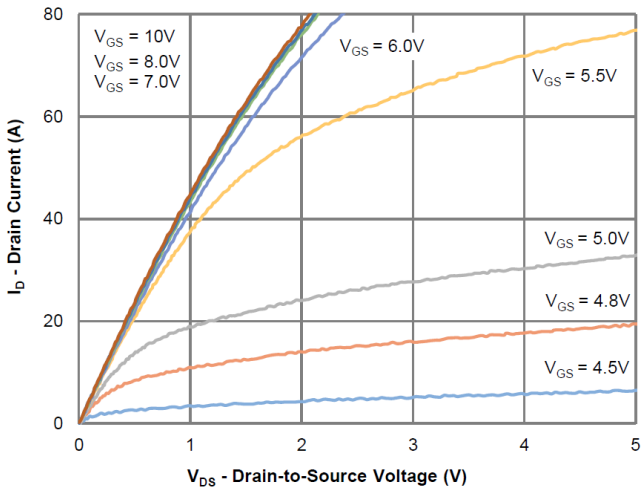


Figure 1: Output Characteristics

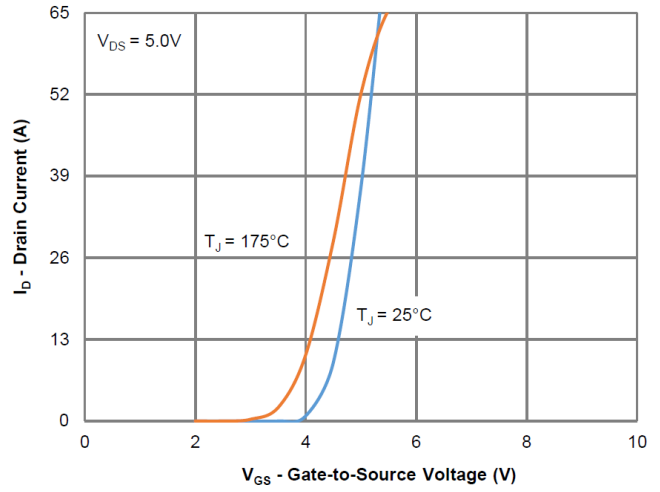


Figure 2: Transfer Characteristics

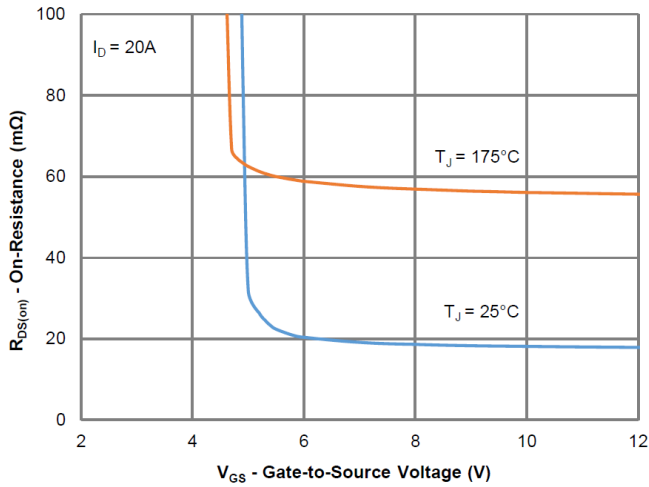


Figure 3: On-Resistance vs. Gate-Source Voltage

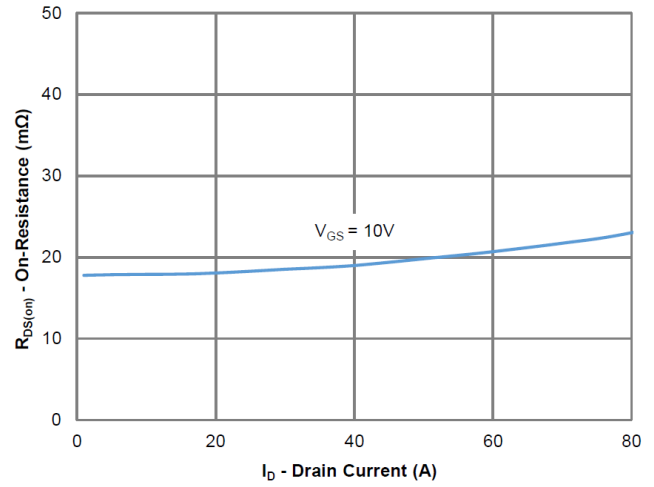


Figure 4: On-Resistance vs. Gate-Source Voltage

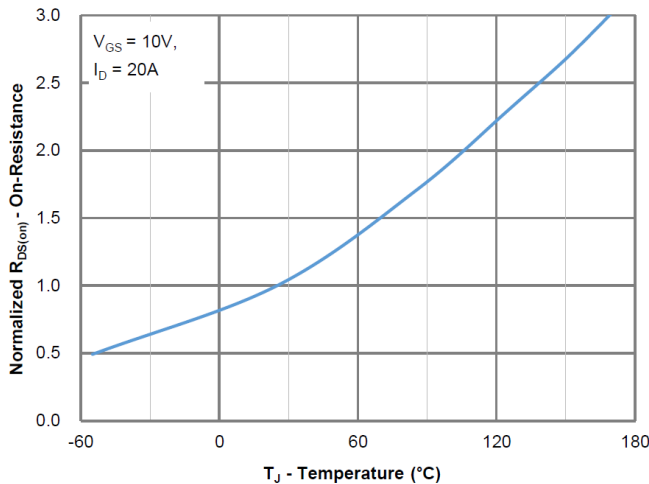


Figure 5: On-Resistance vs. Junction Temperature

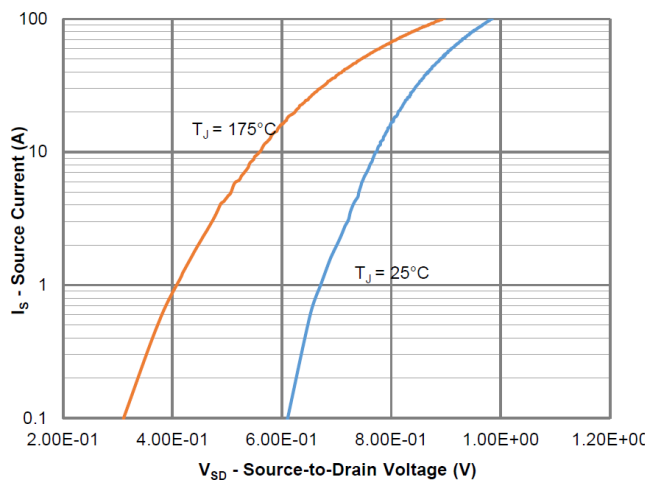


Figure 6: Source-Drain Diode Forward Voltage

Typical Performance Characteristics

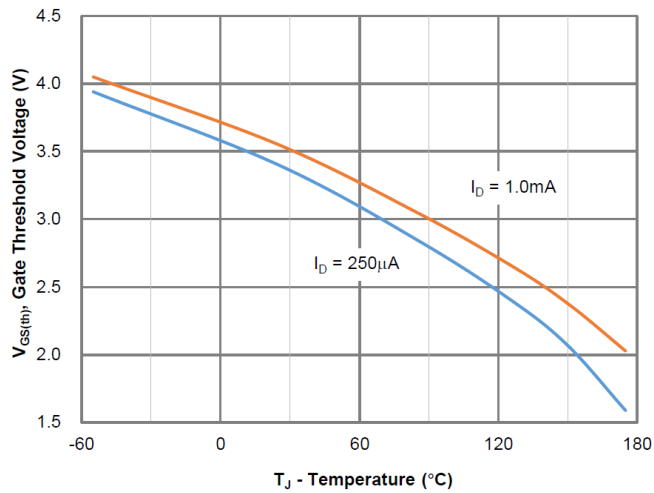


Figure 7: Gate Threshold Variation vs. Junction Temperature

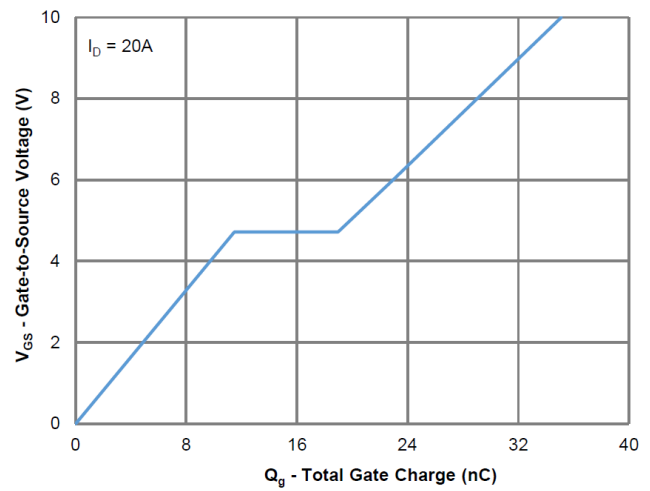


Figure 8: Gate Charge Characteristics

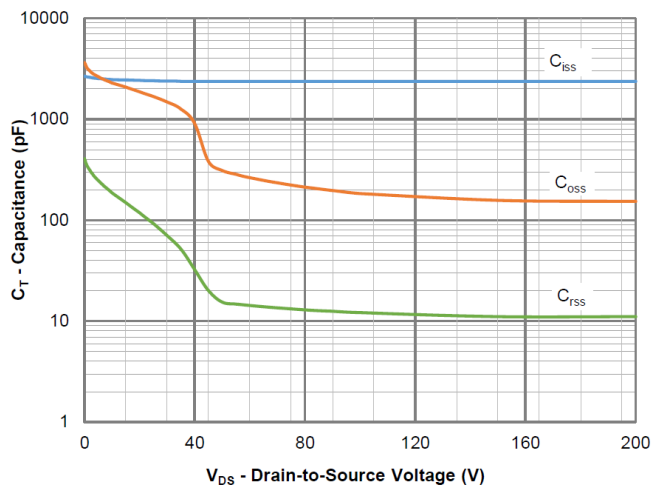


Figure 9: Capacitance Characteristics

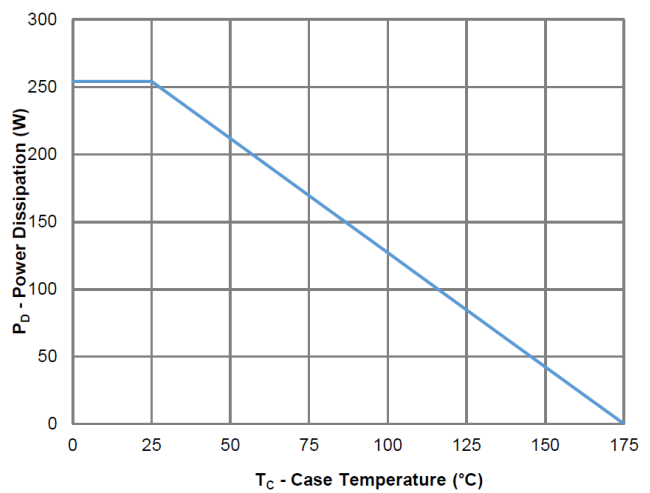


Figure 10: Power Derating

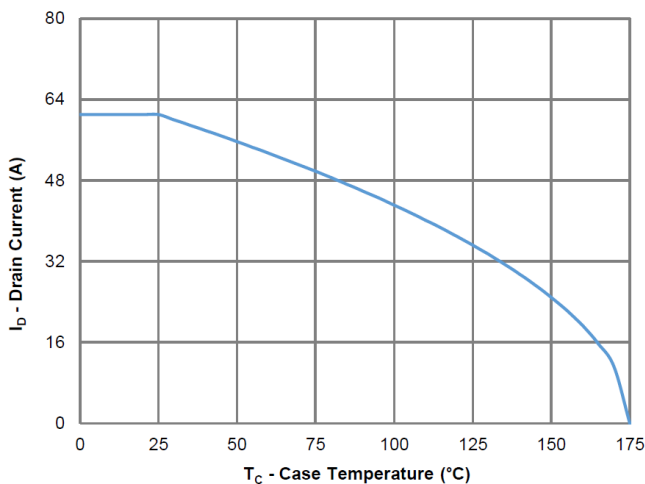


Figure 11: Current Derating

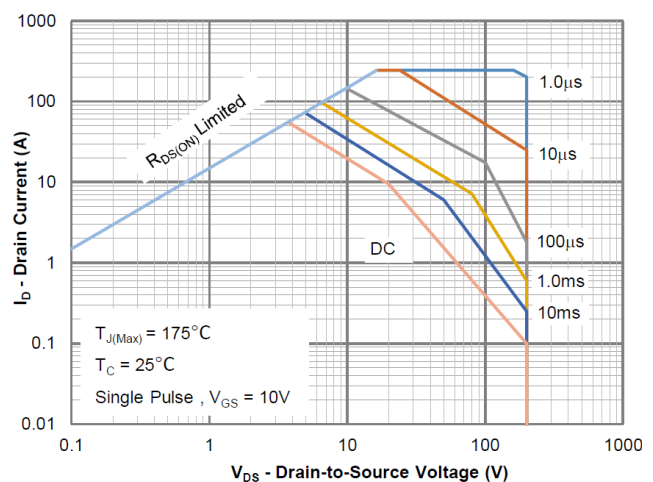


Figure 12: Safe Operating Area



Typical Performance Characteristics

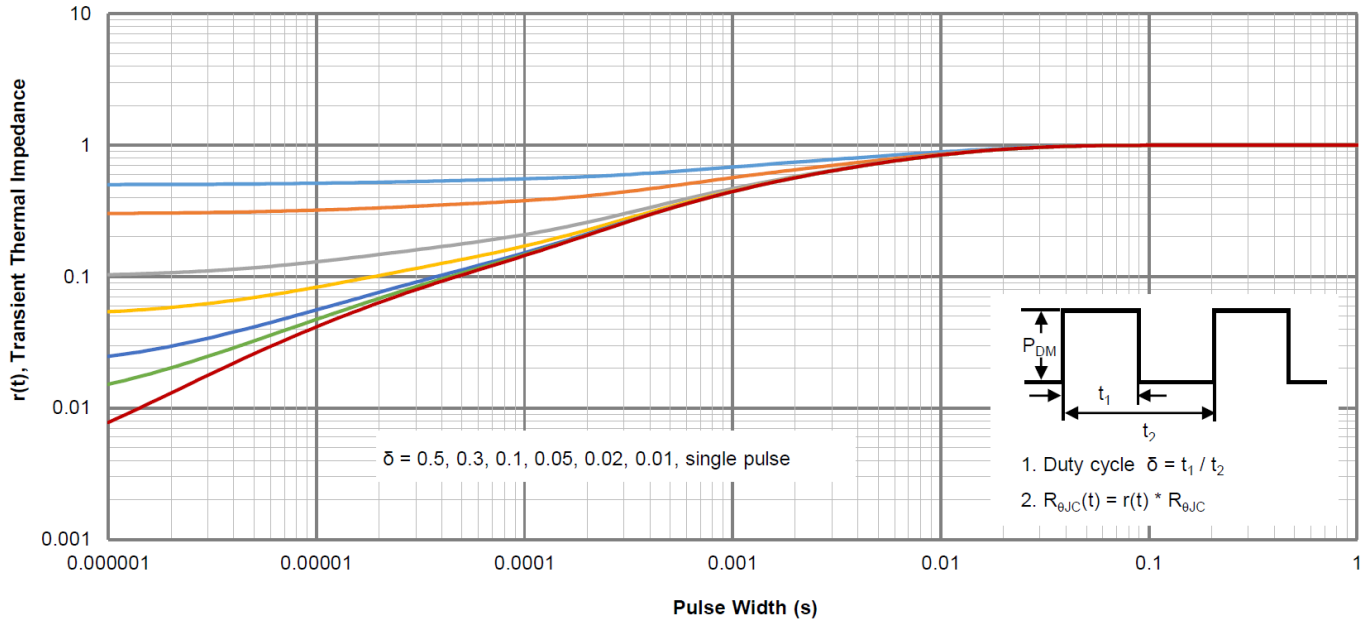
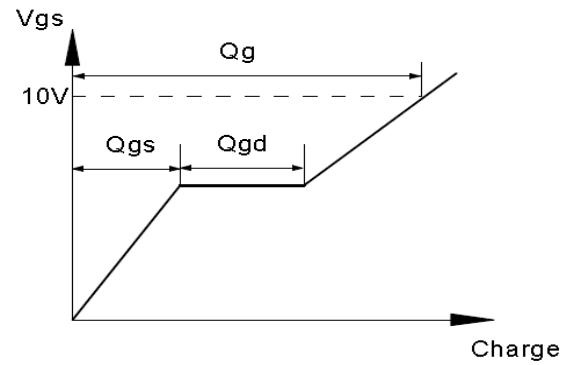
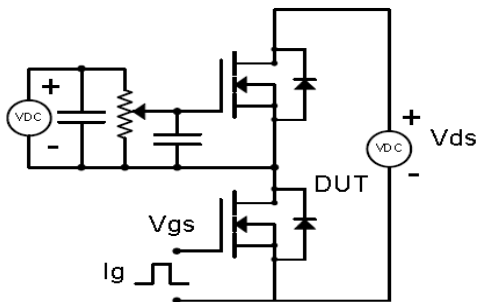
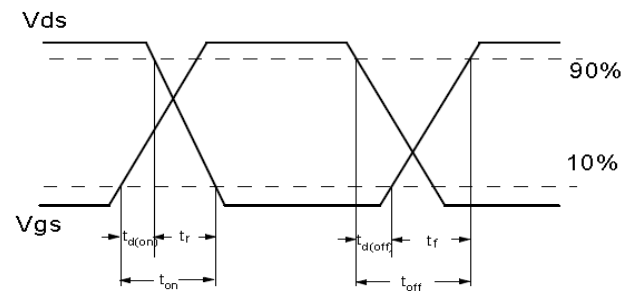
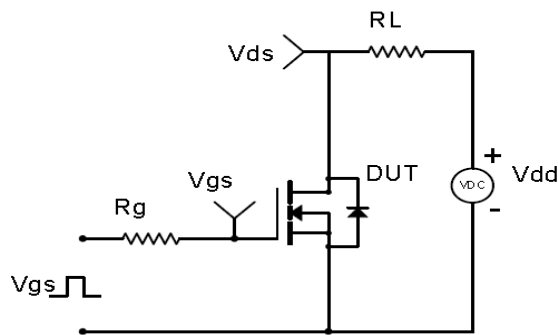
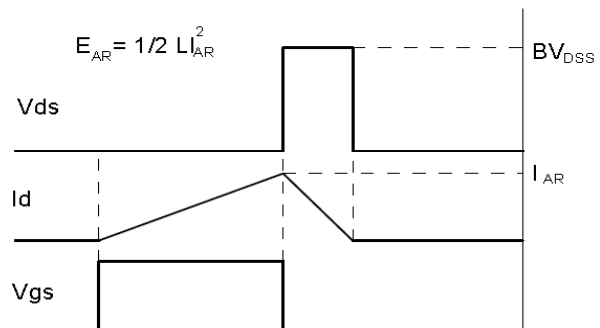
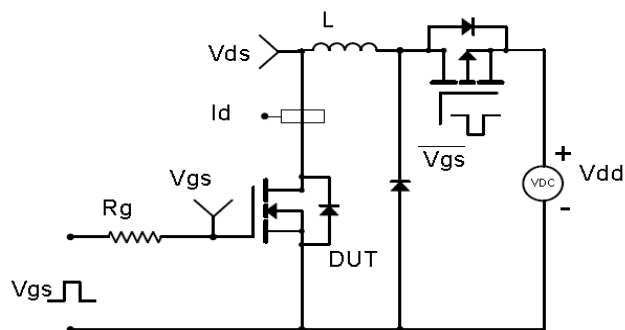
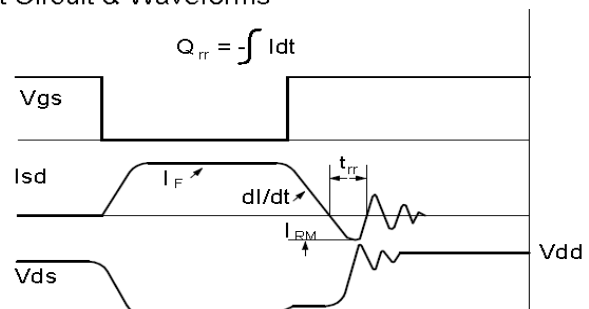
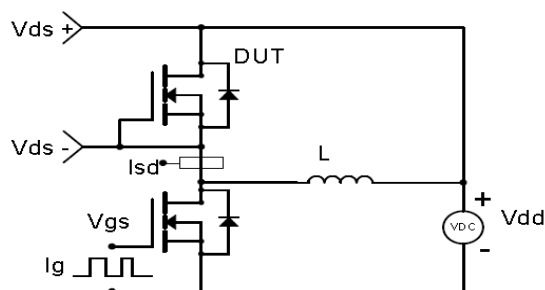
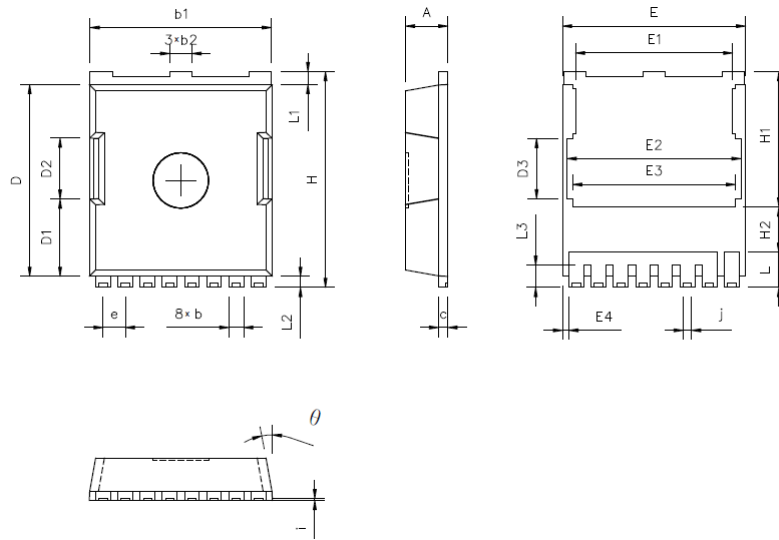


Figure 13: Normalized Maximum Transient Thermal Impedance

Test Circuit & Waveform
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms




Package outline dimensions: TOLL



Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
ø	10° REF		

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