

Product Summary

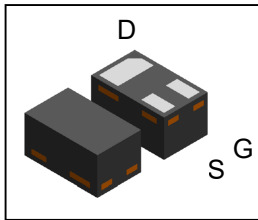
V_{DS} (V)	$R_{DS(on),max}$ (Ω)	I_D (A)
60	1.8@ $V_{GS} = 10V$	0.45

Features

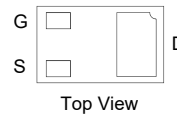
- ❖ High Density Cell Design for Low $R_{DS(ON)}$
- ❖ Voltage Controlled Small Signal Switch
- ❖ Rugged and Reliable
- ❖ High Saturation Current Capability
- ❖ ESD Protected up to 2.0KV(HBM)

Application

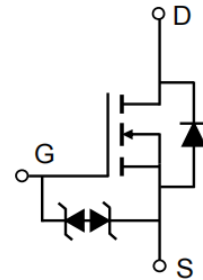
- ❖ Load Switch for Portable Devices
- ❖ Power Management Functions



DFN1006-3L



Equivalent circuit



Absolute Maximum Rating ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($V_{GS}=10V$) ⁽¹⁾	I_D	0.45	A
	I_D	0.31	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	1.3	
Power dissipation	P_D	0.48	W
	P_D	0.31	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽³⁾	$R_{\theta JA}$	200	260	$^\circ\text{C/W}$

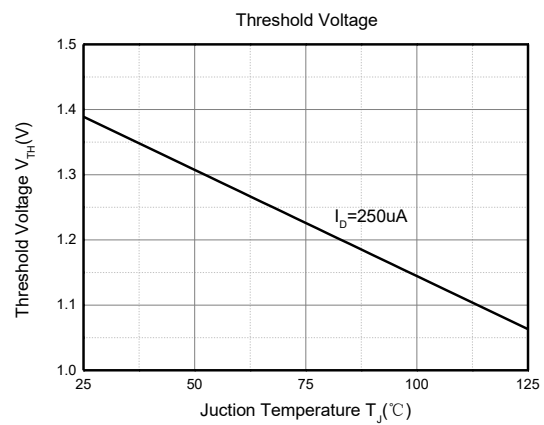
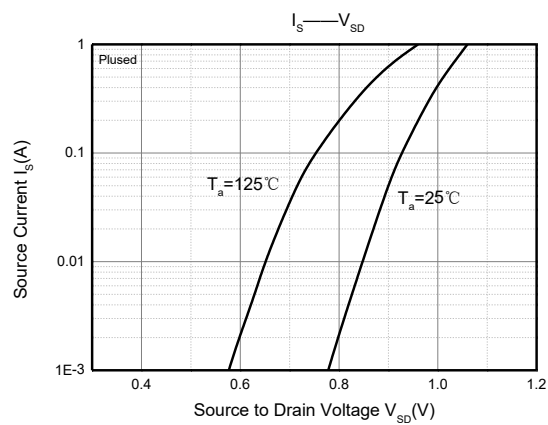
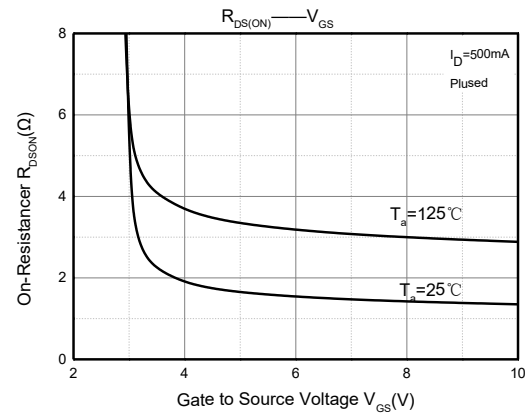
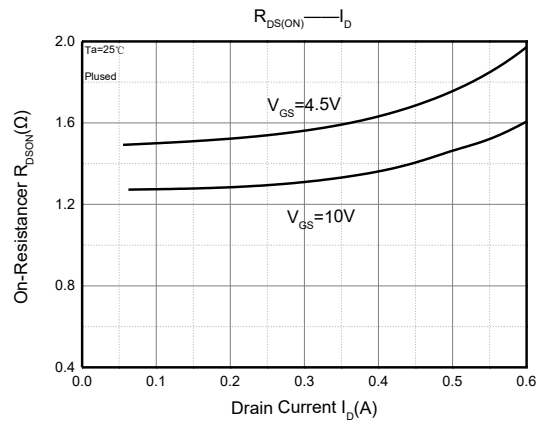
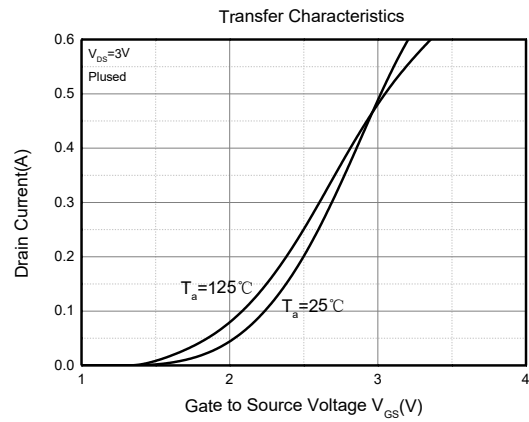
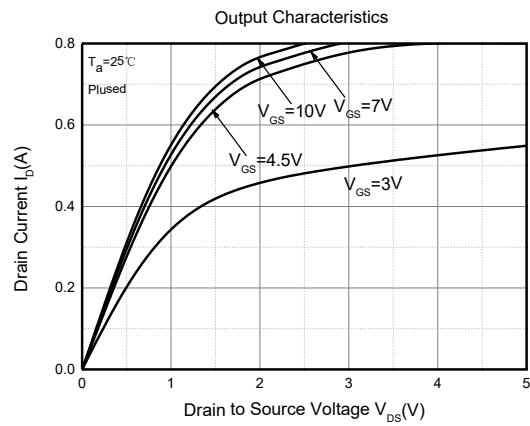
**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter ⁽⁴⁾						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0	1.4	2.0	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 300m A		1.3	1.8	Ω
		V _{GS} = 4.5V, I _D = 100m A		1.5	2.2	
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5.0V, I _D = 200mA		535		mS
Gate resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		42		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 30V, I _D = 300mA V _{GS} = 10V		0.8		nC
Gate-source charge	Q _{gs}			0.22		
Gate-drain charge	Q _{gd}			0.19		
Turn-on delay time	t _{d(on)}	V _{GS} = 10V, V _{DS} = 30V I _D = 300mA, R _{GEN} = 3.0Ω		5.8		ns
Rise time	t _r			2.9		
Turn-off delay time	t _{d(off)}			25		
Fall time	t _f			10.4		
Input capacitance	C _{iss}	V _{DS} = 30V, V _{GS} = 0 V, f = 1 MHz		19		pF
Output capacitance	C _{oss}			7.2		
Reverse transfer capacitance	C _{rss}			3.3		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	I _S = 115mA, V _{GS} = 0V		0.82	1.1	V
Diode Forward Current	I _s	T _A = 25°C			0.45	A

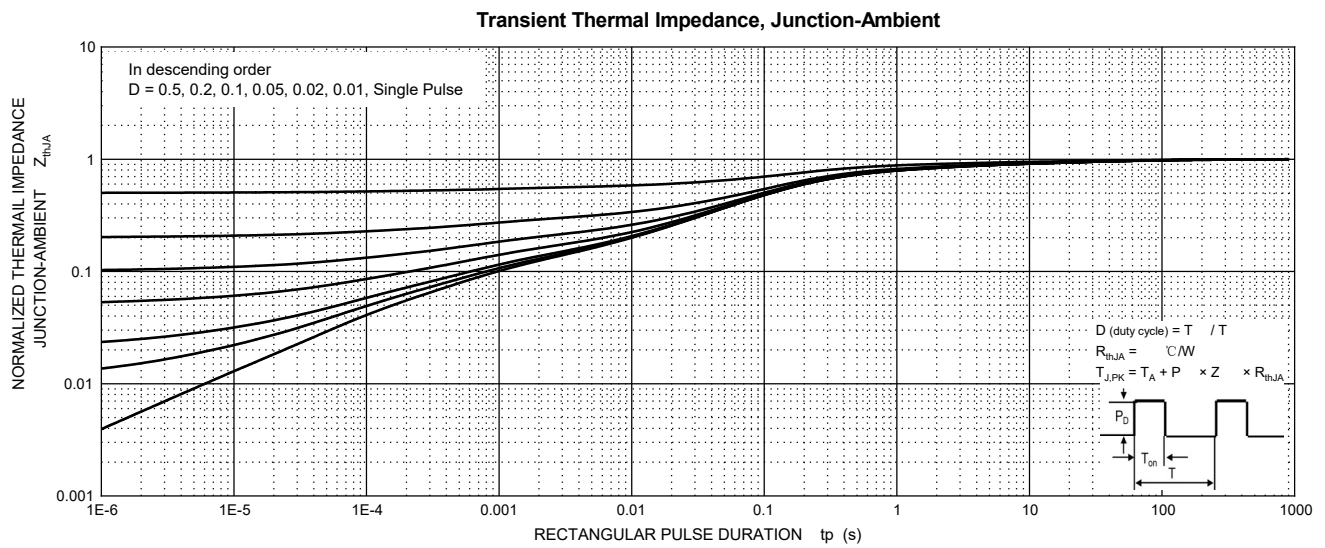
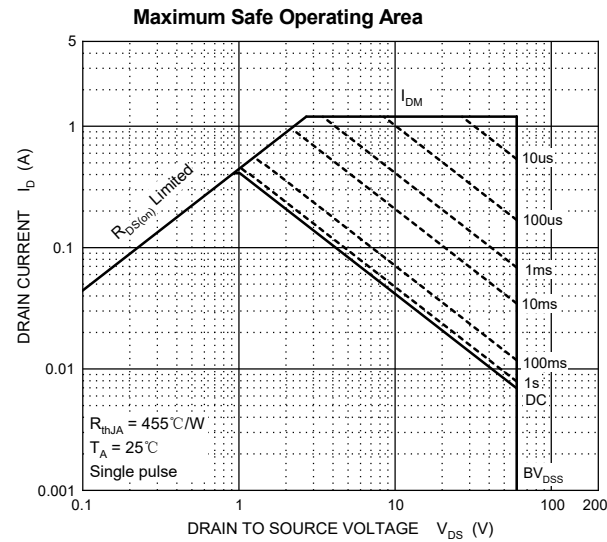
Notes

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

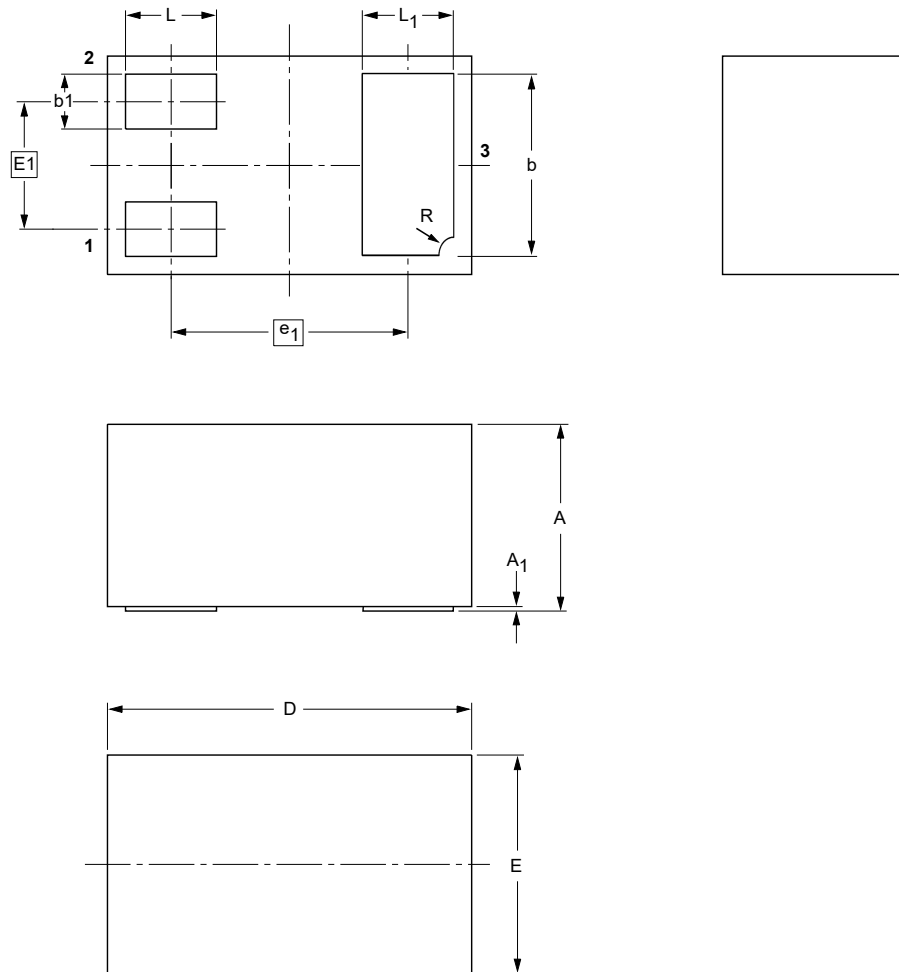
Electrical characteristics diagrams



Electrical characteristics diagrams



Package outline dimensions DFN1006-3L



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b1	b	D	E	E1	e ₁	L	L ₁	R
mm	0.40 0.34	0.05	0.20 0.10	0.55 0.45	1.05 0.95	0.65 0.55	0.35	0.65	0.30 0.20	0.30 0.20	0.15 0.05

Revision History

Revision	Date	Subjects (major changes since last revision)
1	2024-11-06	Release of final version
2	2026-06-12	Update POD

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