

Product Summary

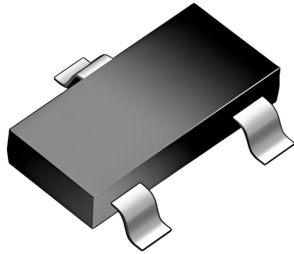
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
30	24@ $V_{GS} = 10V$	6.0

Features

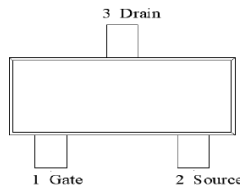
- ❖ High Density Cell Design for Low $R_{DS(ON)}$
- ❖ Voltage Controlled Small Signal Switch
- ❖ Rugged and Reliable
- ❖ High Saturation Current Capability
- ❖ ESD Protected up to 2.0KV(HBM)

Application

- ❖ Load Switch for Portable Devices
- ❖ DC/DC Converter

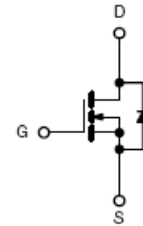


SOT23-3L



PIN Configuration
(Top View)

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 12	
Continuous drain current ($V_{GS}=10V$) ⁽¹⁾	I_D	6.0	A
	I_D	5.0	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	30	
Power dissipation	P_D	2.0	W
	P_D	1.35	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽³⁾	$R_{\theta JA}$	62.5		$^\circ\text{C/W}$

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter ⁽⁴⁾						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	30			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	0.6	0.9	1.5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} =30 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 6 A		18	24	mΩ
		V _{GS} = 4.5V, I _D = 5 A		20	28	
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5.0V, I _D = 6A		30		S
Gate resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		3.2		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 10V, I _D = 5A V _{GS} = 6V		6.8		nC
Gate-source charge	Q _{gs}			2.0		
Gate-drain charge	Q _{gd}			2.3		
Turn-on delay time	t _{d(on)}	V _{GS} = 10V, V _{DS} = 15V R _L = 2.7Ω, R _{GEN} = 3.0Ω		2.8		ns
Rise time	t _r			3.2		
Turn-off delay time	t _{d(off)}			23		
Fall time	t _f			5.0		
Input capacitance	C _{iss}	V _{DS} = 15V, V _{GS} = 0 V, f = 1 MHz		642		pF
Output capacitance	C _{oss}			78		
Reverse transfer capacitance	C _{rss}			53		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	I _S = 1A, V _{GS} = 0V		0.75	1.0	V
Diode Forward Current	I _s	T _A = 25°C			6.0	A

Notes

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

Electrical characteristics diagrams

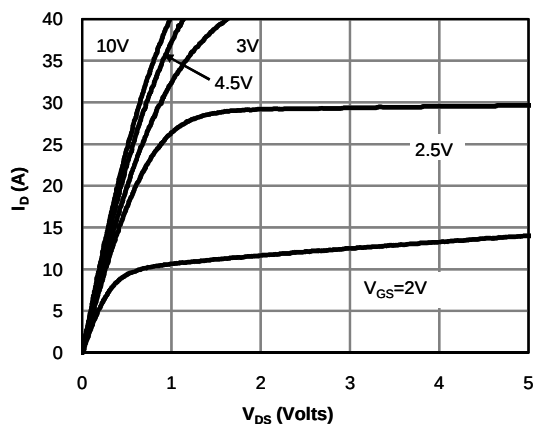


Fig 1: On-Region Characteristics (Note E)

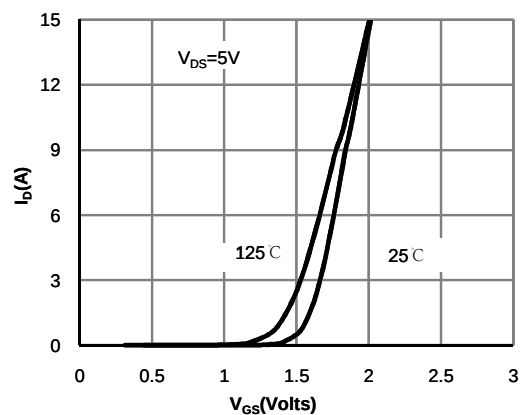


Figure 2: Transfer Characteristics (Note E)

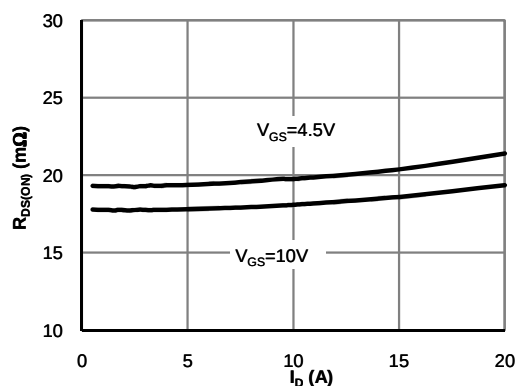


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

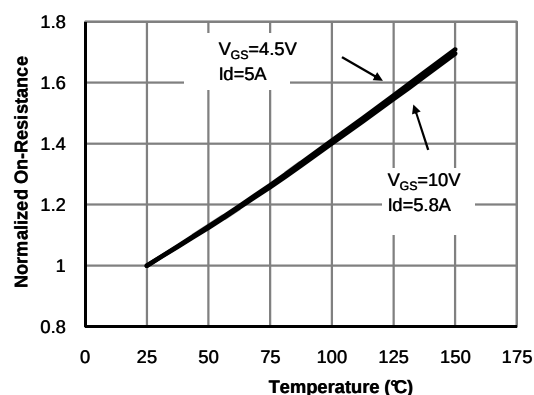


Figure 4: On-Resistance vs. Junction Temperature (Note E)

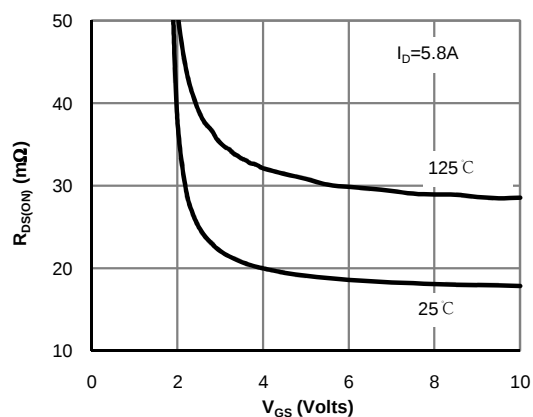


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

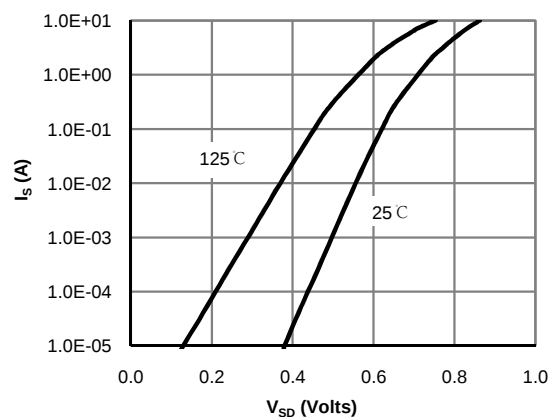
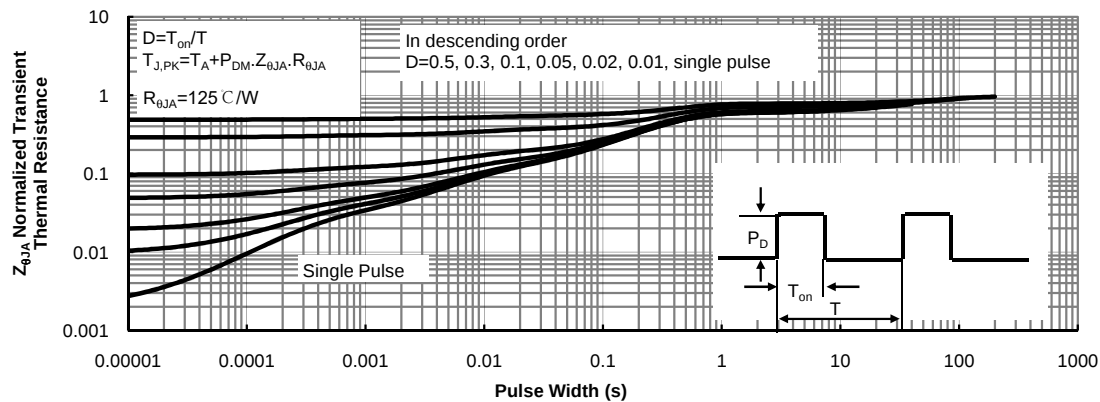
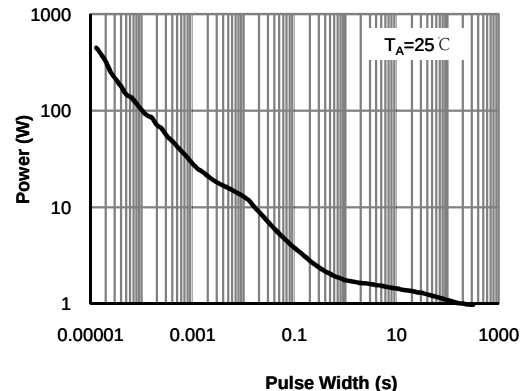
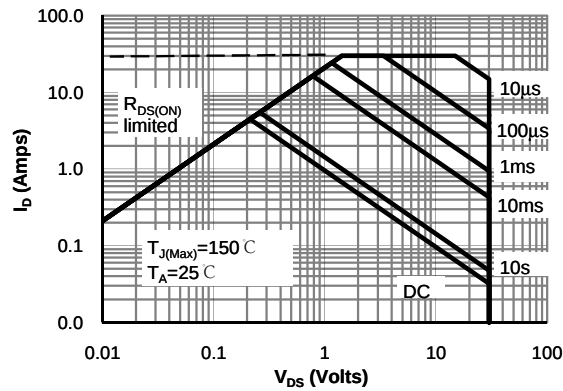
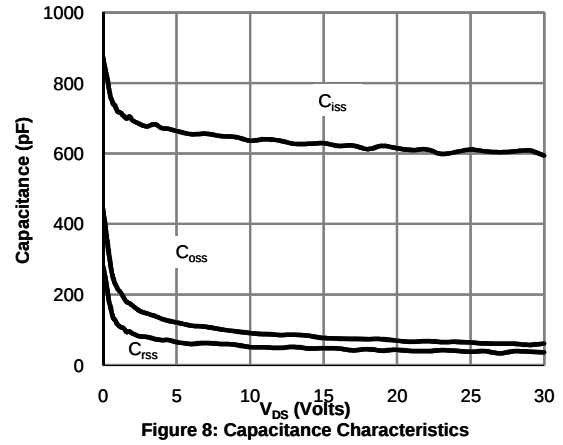
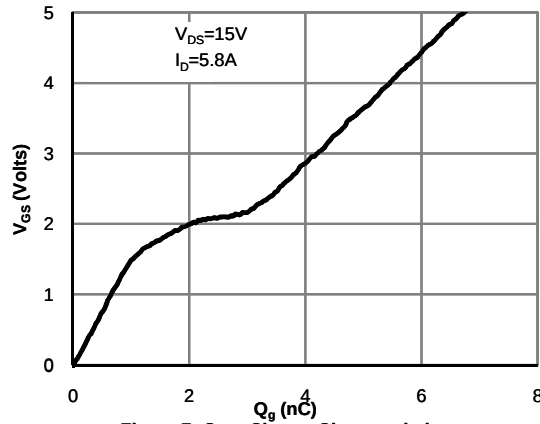
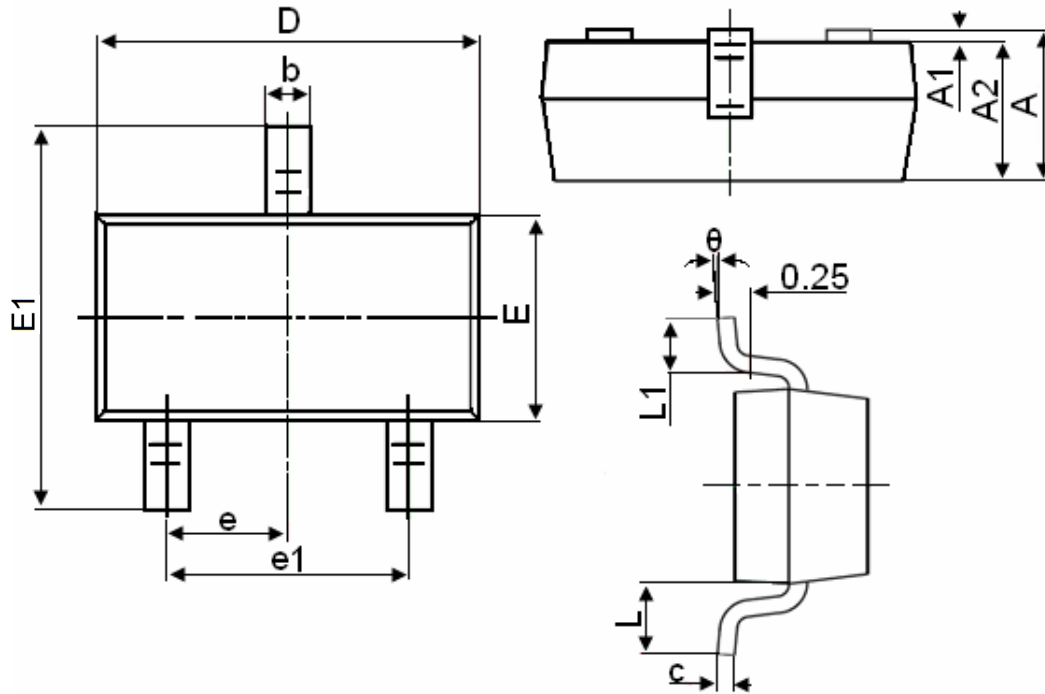


Figure 6: Body-Diode Characteristics (Note E)

Electrical characteristics diagrams



Package outline dimensions SOT23-3L


Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.90	1.150
A1	0.0	0.100
A2	0.9	1.050
b	0.30	0.500
c	0.08	0.150
D	2.80	3.000
E	1.50	1.700
E1	2.65	2.950
e	0.950 TYP	
e1	1.8	2.000
L	0.55 REF	
L1	0.3	0.500
θ	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified.
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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