

Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
-20	33 @ $V_{GS} = -4.5V$	-4.9

Features

- ❖ Fast Switching
- ❖ Low On-Resistance
- ❖ Low Gate Charge

Application

- ❖ Load Switch
- ❖ Motor Control
- ❖ Power Management

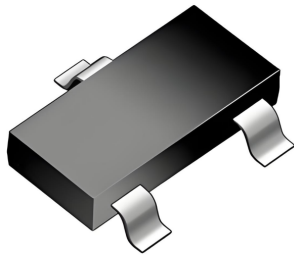
General Information

Shipping

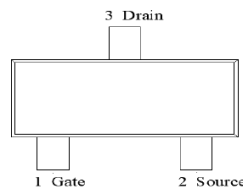
- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

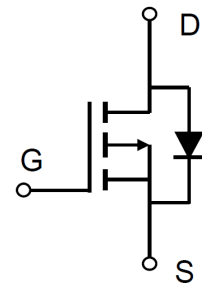


SOT-23



PIN Configuration
(Top View)

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	-20	V
Gate-source voltage	V_{GS}	± 8	
Continuous drain current ($V_{GS}=-4.5V$) ⁽¹⁾	I_D	-4.9	A
	I_D	-3.9	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-19.5	
Power dissipation	P_D	1.1	W
	P_D	0.73	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽³⁾	$R_{\theta JA}$	85	110	$^\circ\text{C/W}$

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter ⁽⁴⁾						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.4	-0.6	-1.0	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V			-1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -4.1 A		27	33	mΩ
Forward transconductance	g _{fs}	V _{DS} = -5.0V, I _D = -4.1A		8.0		S
Gate resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		21		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = -10V, I _D = -4.1A V _{GS} = -4.5V		7.3		nC
Gate-source charge	Q _{gs}			1.0		
Gate-drain charge	Q _{gd}			1.6		
Turn-on delay time	t _{d(on)}	V _{GS} = -4.5V, V _{DS} = -10V I _D = -4.1A, R _{GEN} = 3.0		6.9		ns
Rise time	t _r			15		
Turn-off delay time	t _{d(off)}			72		
Fall time	t _f			36		
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz		820		pF
Output capacitance	C _{oss}			114		
Reverse transfer capacitance	C _{rss}			93		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	I _S = -2.0A, V _{GS} = 0V		-0.71	-1.2	V
Diode Forward Current	I _s	T _A = 25°C			-4.9	A

Notes

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

Electrical characteristics diagrams

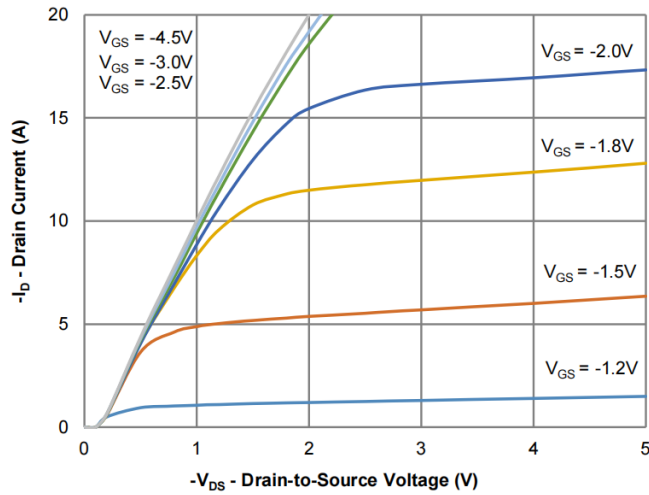


Figure 1: Output Characteristics

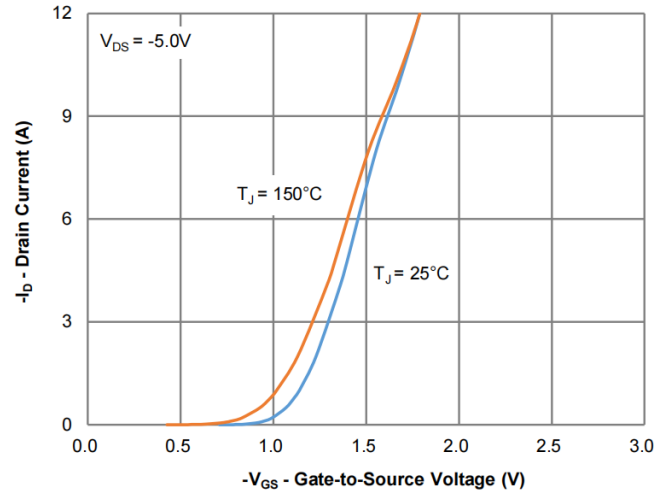


Figure 2: Transfer Characteristics

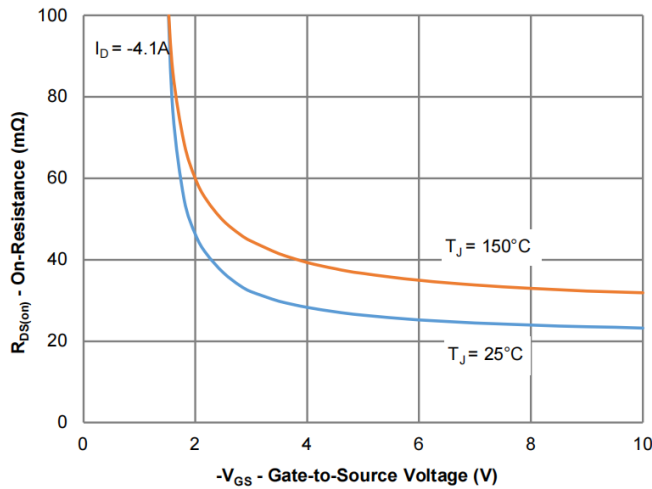


Figure 3: On-Resistance vs. Gate-Source Voltage

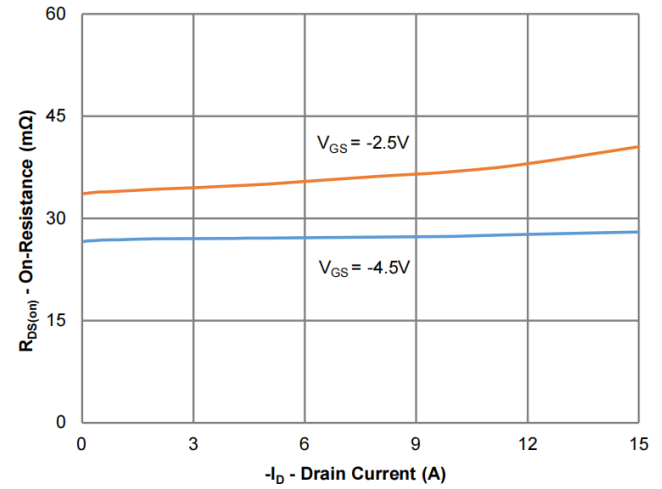


Figure 4: On-Resistance vs. Gate-Source Voltage

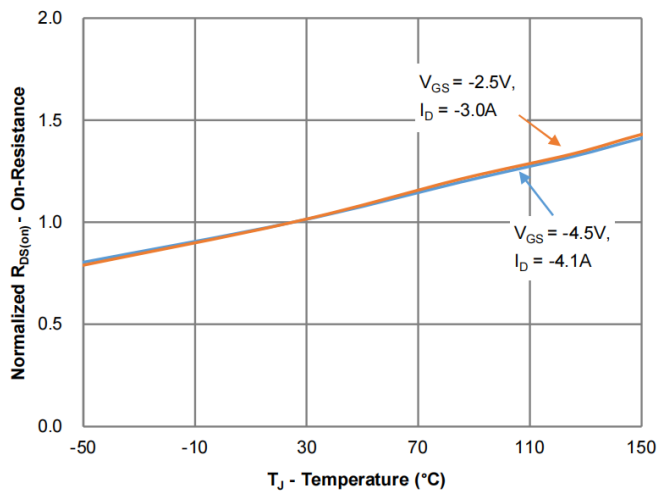


Figure 5: On-Resistance vs. Junction Temperature

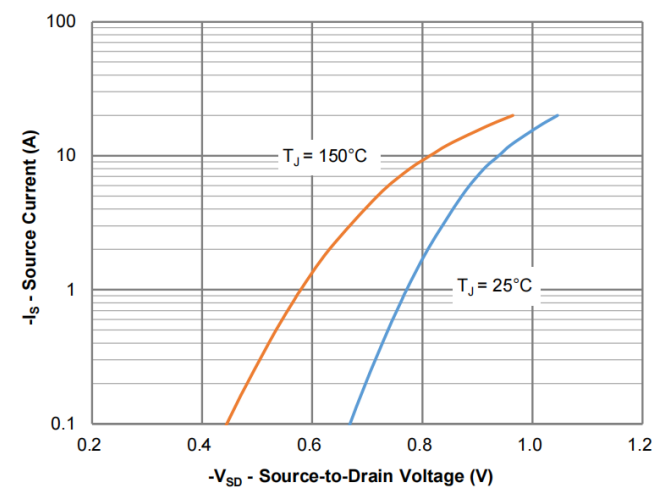


Figure 6: Source-Drain Diode Forward Voltage

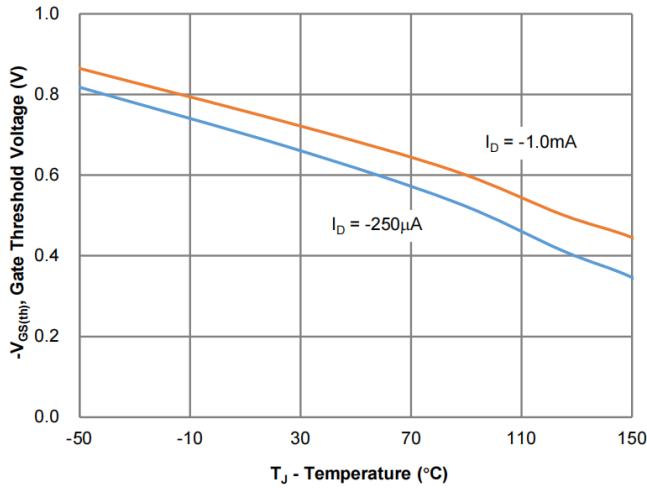


Figure 7: Gate Threshold Variation vs. Junction Temperature

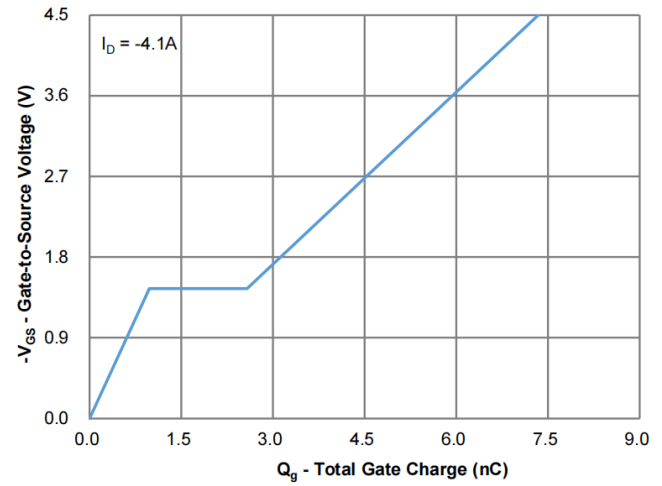


Figure 8: Gate Charge Characteristics

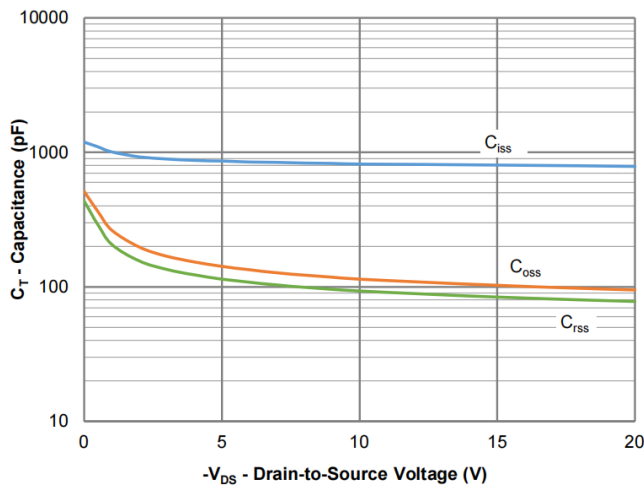


Figure 9: Capacitance Characteristics

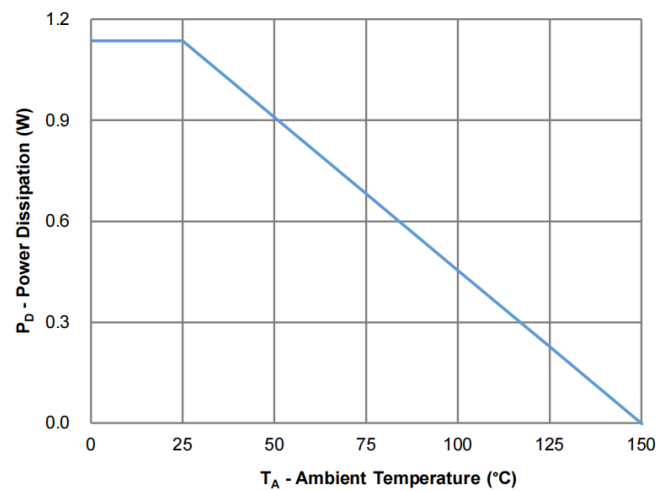


Figure 10: Power Derating

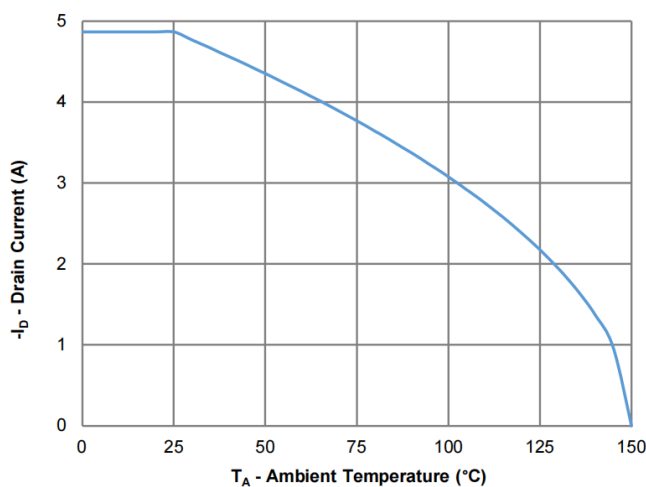


Figure 11: Current Derating

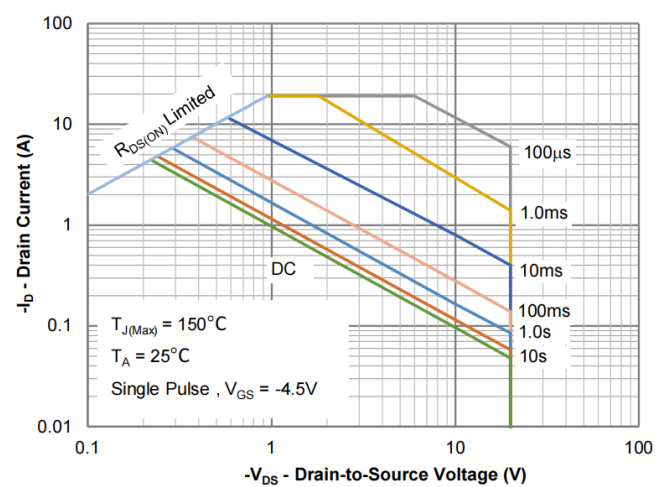


Figure 12: Safe Operating Area

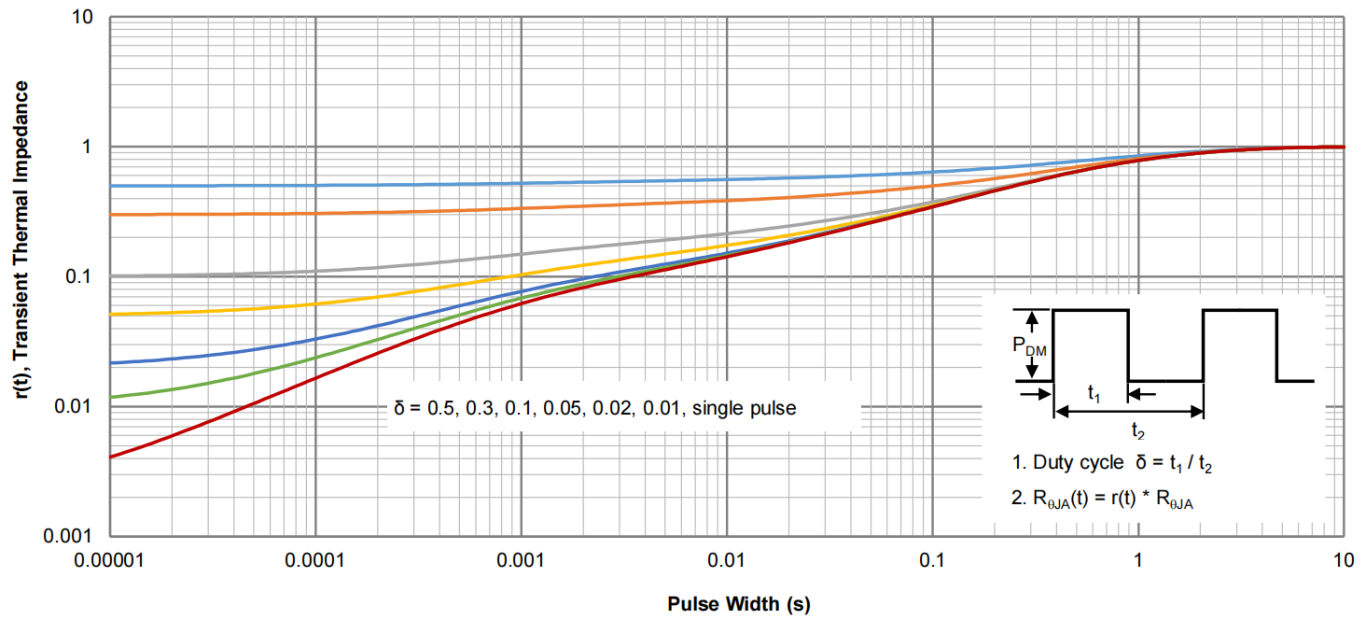
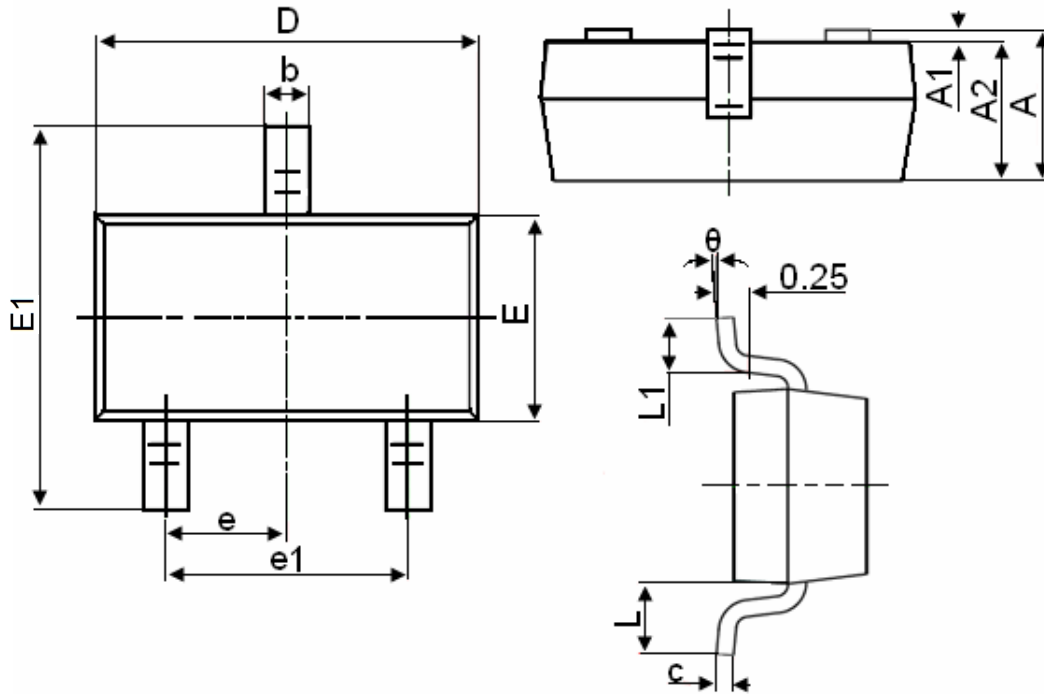


Figure 13: Normalized Maximum Transient Thermal Impedance

Package outline dimensions SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.90	1.150
A1	0.0	0.100
A2	0.9	1.050
b	0.30	0.500
c	0.08	0.150
D	2.80	3.000
E	1.20	1.400
E1	2.2	2.550
e	0.950 TYP	
e1	1.8	2.000
L	0.55 REF	
L1	0.3	0.500
θ	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified.
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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